Modeling and simulation of subthreshold characteristics of fully-depleted recessed-source/drain UTB SOI MOSFETs including substrate induced surface potential effects

A dissertation submitted in partial fulfillment of requirement for the Degree of

Master of Technology

in

VLSI Design and Embedded Systems

by

AJIT KUMAR

Roll No. 212EC2134

to

Department of electronics and communication engineering

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA (INDIA)

May 2014

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Department of Electronics and Communication Engineering

National Institute of Technology

Rourkela (India)

CERTIFICATE

This is to certify that the thesis entitled "**Modeling and simulation of sub-threshold characteristics of fully-depleted recessed-source/drain UTB SOI MOSFETs including substrate induced surface potential effects**" being submitted by **AJIT KUMAR** bearing Roll No. 212EC2134 to Electronics and Communication Department in National Institute of Technology Rourkela is a bona fide work carried out by him under my supervision and guidance.

To the best of my knowledge the research work presented in the dissertation has not been reported in part or full at any other university or institute for fulfillment of any Diploma or Degree.

Dr. Pramod K. Tiwari

Rourkela — Assistant Professor, Department of ECE

May 2014 — National Institute of Technology Rourkela (India)

Dedicated to my high school J. N. V. Nawada (Bihar) and the teachers

for their dedication and selflessness

ABSTRACT

With the introduction of Silicon-on-Insulator MOSFET, the device technology has witnessed the scaling from tens of micrometer to tens of nanometer. It has gone through multiple successful structural modifications and still is in research to reintroduce it into sub 10nm era. In the work the recessed source/drain structure is being explored down to 10nm channel length.

A two-dimensional channel surface potential of Re-S/D SOI MOSFET has been developed using evanescent model with substrate induced surface potential effects. The channel potential is broken into one-dimensional long-channel potential and two-dimensional short-channel effective potential. The front and back surface of channel are studied for dominance in current drive capacity and threshold voltage has been formulated accordingly. To model the substrate induced surface potential (SISP) effects at substrate/buried-oxide interface a one-dimensional Poisson's equation has also been solved in the substrate region. The generalized surface potential model together with SISP effects consideration improves the accuracy of the threshold voltage and subthreshold characteristic model.

MATLAB has been utilized to find the numerical model results for variations in the device parameters and the corresponding results have been verified using device simulator ATLAS^{TM} from Silvaco. The model and simulation results have been plotted together and accuracy of model was verified.

ACKNOWLEDGENENT

My first and foremost gratitude goes to my project supervisor P. K. Tiwari for his overwhelming support and encouragement throughout the work. His suggestions and constant efforts have been proved to be extremely useful in improving the quality of the work. The discussion with him related to the work has been proved to be the most invaluable source of learning for me. I have strong wish to adhere his qualities and determination.

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Finally, I thank GOD for blessing me with loving and supporting parents and family members as I would not have even dreamed of pursuing higher education without their love, affection and support.

Ajit Kumar

Dept of ECE, NIT Rourkela

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LIST OF SYMBOLS

n_i	Intrinsic carrier concentration of Si
K	Boltzmann constant
T	Temperature in Kelvin
$\varepsilon_{ox}, \varepsilon_{si}, \varepsilon_b$	Dielectric constants associated with gate-oxide, Si-body, and BOX respectively
$t_{ox}, t_{si}, t_b, t_{rsd}$	Thickness associated with gate-oxide, Si-channel, BOX, and source/drain depth in BOX respectively
C_{ox}, C_{si}, C_b, C_r	Capacitance per unit area associated with gate-oxide, Si-channel, buried-oxide, and between recessed S/D and back-surface of channel respectively
L	Channel length of the device
d_b	Overlap length of buried-oxide with recessed-s/d
t_{rsd}^*	Effective thickness of recessed-s/d in buried-oxide
N_a, N_{sub}, N_d, N_s	Doping concentration associated with Si-body, substrate, drain, and source respectively
$V_{fb1}, V_{fb2}, V_{fb3}$	Flat band voltage associated with front-gate, source/drain-back channel surface, and substrate-back channel surface respectively
V_g, V_s, V_d, V_{sub}	Voltage applied to gate, source, drain, and substrate respectively
$V_{ds} = V_d - V_s$	Drain to source voltage

V_{bi}	Built-in potential associated with source/drain to channel
E_{s1}, E_{s2}, E_{s3}	Electric field at Si-SiO_2 interface below the gate, Si-SiO_2 interface above the buried-oxide, and Substrate-SiO_2 interface below the buried-oxide respectively
$\varphi(x,y), \Psi(x)$	Potential distribution of Si-body (Channel), and substrate respectively
Φ_F, Φ_{sub}	Fermi potential of Si-body, and substrate respectively

LIST OF ABBREVIATIONS

Re-S/D: Recessed-Source/Drain

UTB: Ultra-thin body

SOI: Silicon on Insulator

SISP: Substrate induced surface potential

DIBL: Drain induced barrier lowering

BOX: Buried-oxide

SCE: Short channel effect

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 History of Machines

Human history is actually a relationship between human and machine. Probably wood and clay were among the first few resources to develop a variety of useful tools which took shape of wheel, pot, weapon and other similar basic tools. These primary inventions were the reason which established human dominance on the earth and put us on track of civilization and race for development. Then human entered into Stone Age leading to a variety of powerful tools and some of the world largest man-made structures like the Pyramid of Giza. Near 3300BC the metals were introduced in human history with the start of Bronze Age [1-2]. All of these resources have been being explored in every sphere of human life and their applications have increased radically instead of saturation. Further after being used in crude form for around 5000 years the petrochemical substance got revolutionized in 20^{th} century owing to the modern refinery.

However in 20^{th} century human hunger for development gave rise to exploration of two most amazing substances nuclear-active element and semiconductor. Both of them need very high expertise to develop and utilize them safely. On one side nuclear energy is the driving force of development of urban life, whereas on the other hand Semiconductor technology has given rise to the most sophisticated machines which work at very high speed together with extreme precision. Figure 1.1 depicts a p-type Si with Phosphorous as doping which can be considered as

the simplest semiconductor structure but basic building block of all semiconductor devices. Today from pocket calculator to the supercomputer used in satellite monitoring has become largely dependent on semiconductor materials.

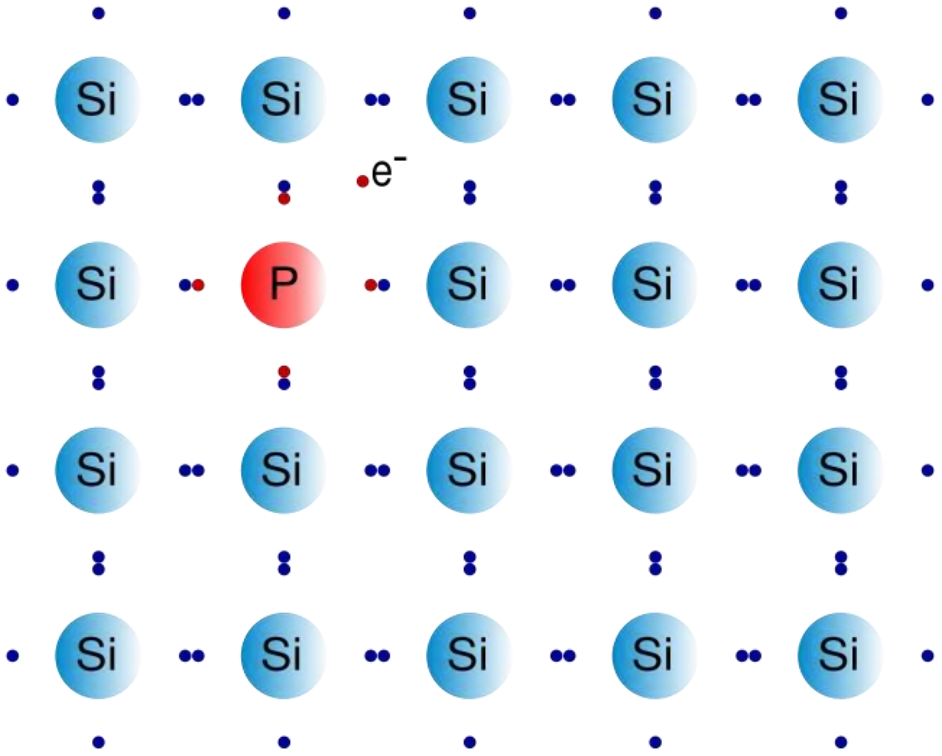

Figure 1.1 Phosphorous-doped Silicon (p-type)

1.2 Semiconductor Materials

In 19th century some of the unusual properties were observed in a few substances like Ag_2S and Cu_2S [3-4]. Among these temperature coefficient for resistance being negative, rectification behavior, and sensitivity to light observations leads to the terminology

'Semiconductor' which was later explained by a separate branch of science called Solid-State Physics. It deals with purification, impurity implantation, semiconductor-semiconductor junction, metal- semiconductor junction, application of light etc. with their behavior in different region of operation. After exploration of Germanium, Silicon, gallium-arsenide etc. now a day focus is being given to organic semiconductor devices, however the decades of research in the area of conventional semiconductors Si, Ge, and GaAs has made these substance an important part of semiconductor technology which cannot be replaced for long time.

1.3 Semiconductor Devices

The semiconductor diode was developed in early 1990's and became extremely popular over vacuum tube because of small size and high stability in rectification. The successful demonstration of transistor was carried out in 1947 at Bell Laboratories [3]. The commercial production of junction transistors for portable radios was started by Texas Instruments in 1954. Soon junction transistors replaced vacuum tube in multiple applications. The concept of Field Effect Transistor was developed to improve the reliability of the device using passivation of surface with SiO_2. The basic structure of Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is shown in Figure 1.1. An n-type MOSFET consists of an n-type source and an n-type drain over p-type substrate which provides isolation due to reverse-biased p-n diodes nature. The region between source and drain is covered by metal or poly-crystalline gate, and is separated from channel by gate-oxide. The continuous research in semiconductor devices and its application in technological growth reinforced each other and soon scaling of the semiconductor devices became most challenging task.

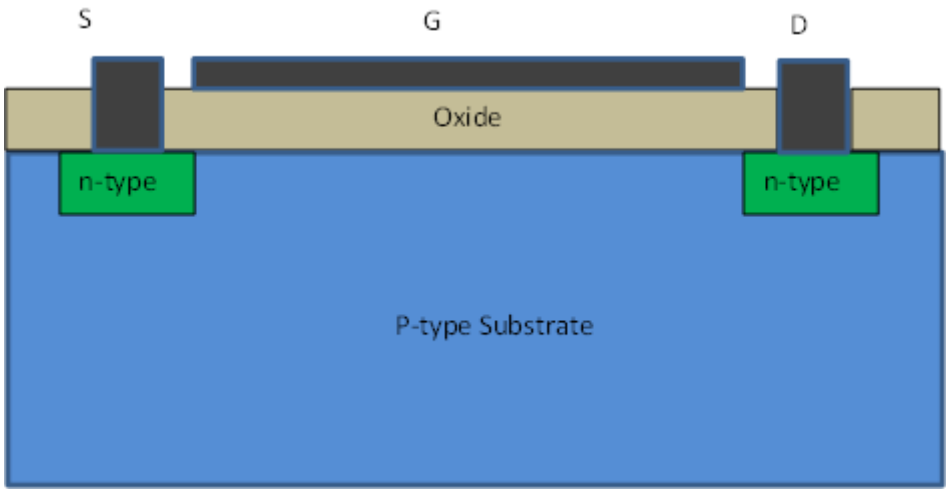

Figure 1.2 Conventional MOSFET

1.4 SOI MOSFET and Device Scaling

According to the statement of Gordon E. Moore, "Moore's law" was coined around 1970 whose basic idea can be represented by Figure 1.2 [5]. However a number of issues like leakage current and parasitic capacitances of MOSFETs arise upon scaling Conventional MOSFET in nm range. From early 80's itself the drawback of MOSFET has been reported while attempting reduction in device dimension. In 1974 Dennard et al. [6] showed the need of high doing with diminished dimension. Subsequently the need of high doping and consequent degrade in mobility was reported in [7-10] which causes low drive current capacity. Threshold voltage fluctuation is reported in [11] associated with conventional MOSFET. Hence Conventional MOSFET failed in following Moore's law. To counteract the issues Silicon-on-Insulator technology was introduced in which a semiconductor layer such as silicon or germanium is formed on an insulator layer e.g., SiO_2 buried oxide. The performance of SOI MOSFETs has been evaluated in numerous literatures on different grounds. SOI MOSFETs takes advantage of

improved short channel effect with ultrathin body [12-13]. One of the biggest advantages of SOI MOSFET with respect to Conventional MOSFET is the elimination of leakage paths [14]. SOI structure also provides other advantages in term of reduced parasitic capacitance, excellent gate control etc. [4] and [15]. Ref. [13] has also found SOI with Mesa isolation to be less dependent from drain voltage, better gate control and less punch through. Adan et. al [16] has studied SOI MOSFET for non-uniform channel doping and floating body effects. Also, undoped or lightly doped thin-body MOSFET has been reported in [17] to have better electrostatic behaviour at short gate lengths. The cuts off in substrate leakage current paths and reduced parasitic capacitances have made SOI MOSFET a very attractive option in both analog and digital applications [4] and [15]. Further SOI MOSFETs has been being studied with quantum effects which make it clear that the structure is fully capable of functioning at around 10nm device dimension [18-20].

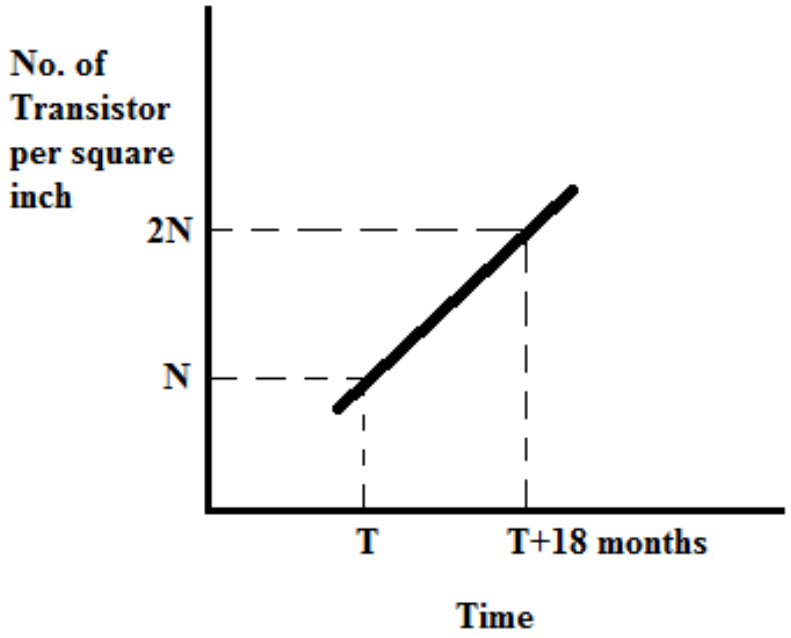

Figure 1.3: Moore's Law demonstration

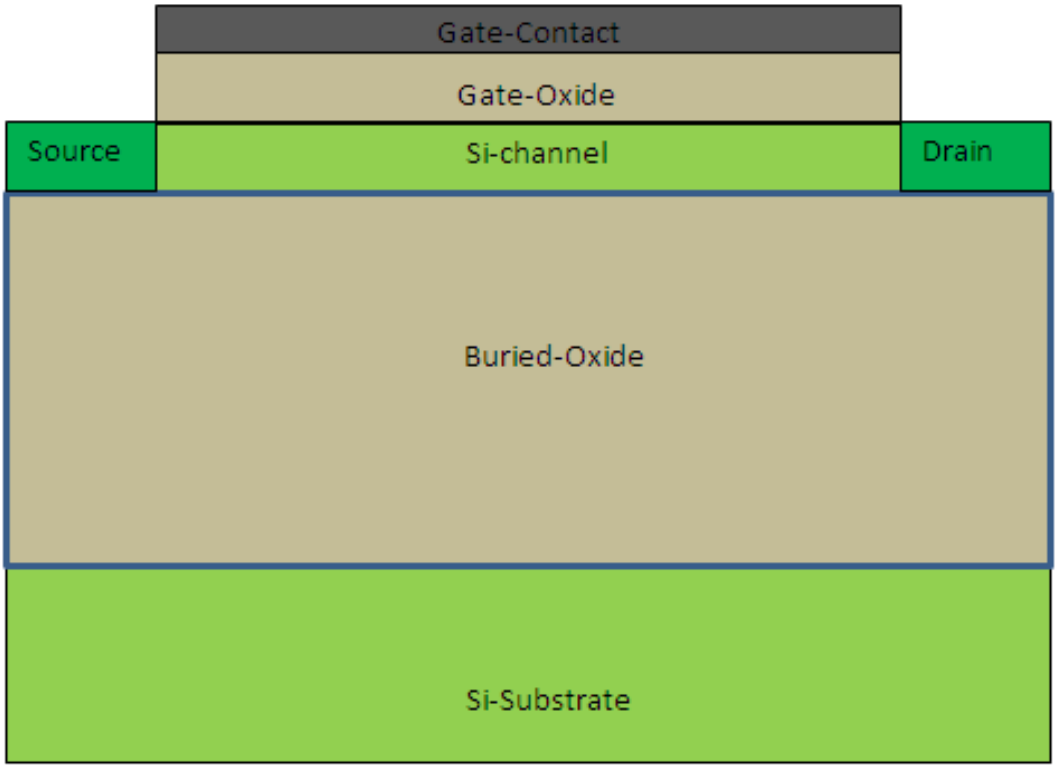

Figure 1.4: Conventional SOI MOSFET

1.5 Fully-Depleted Channel

UTB is the further dig in ETB device. With device being scaled down, a corresponding scaling in channel thickness is also followed to control SCE and threshold dipping [5]. In case of UTB the channel thickness of 2 to 5 nm may be considered. Further due to this thickness the channel is extremely controlled by gate. Thus whole channel region gets depleted with application of gate voltage and hence improve the drive current capability, however it can not be scaled below some limit in the present device theory because of the decrease in drain current and tunneling though it [21-23].

1.6 Scope of the Thesis

The remaining part of the work is being broadly divided into five chapters each with multiple sub-sections. Each chapter can be summarized as below.

CHAPTER 2- It is Literature Review section in which the proposed structure of Re-S/D SOI MOSFETs has been shown with the device parameters symbols which is followed by previous works carried out are briefed. The flaws of previous models have been explained and their corrections were suggested to be incorporated in the present model.

CHAPTER 3- This part begins with Poisson's Equation for the channel region together with the boundary conditions. Then solution of Poisson's Equation is presented to obtain generalized 2 D channel potential. Further to explain the nature of ΔV term associated in the channel potential modeling of SISP effects has been presented. The results were demonstrated in the form of plots.

CHAPTER 4- Using the channel potential obtained in previous chapter, the threshold voltage of Re-S/D SOI MOSFET was extracted. The inversion condition is mentioned in this section to achieve threshold. Then the results were plotted for variation in the device parameters.

CHAPTER 5- In this section subthreshold current and subthreshold swing was defined and corresponding models were developed using two-dimensional surface potential of channel region. The numerical results were plotted to observe the variation with device parameters.

CHAPTER 6- This is the final section of the core thesis in which the results and findings were highlighted. The benefits of present model with respect to the targets set in chapter 2 are briefed and light is thrown on the related future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Re-S/D vs. Elevated-S/D SOI MOSFET: An Introduction

The SOI technology has saved Moore's law for almost a decade but the technology appeared to be failing 2010 onwards. Upon aggressive scaling the SOI MOSFET suffers from high source/drain and series resistance and low drive current due to channel thickness of sub 10nm [24-27]. The hunger of shrinking size of various electronic devices has provoked the proposal of multiple structures e.g., DG [28-29], TG [30] and GAA FETs and thus SOI technology is being threatened which may cause loss of the advantages of the structural and research associated. However two different modifications were proposed in favor of SOI MOSFET. One of them adds an elevated source/drain and in other one a recessed source/drain is implemented. Elevated source/drain structure as shown in Figure 2.1, and recessed-source/drain is shown in Figure 2.2. Both of them provide wide area for source/drain and hence reduce the source/drain series resistance and increase the drive current capability. Both the structures have been researched widely and patented with fabrication methods [31-32]. Though elevated structure reduces the series resistance but reported to be lagging at many levels with respect to Re-S/D SOI MOSFETs.

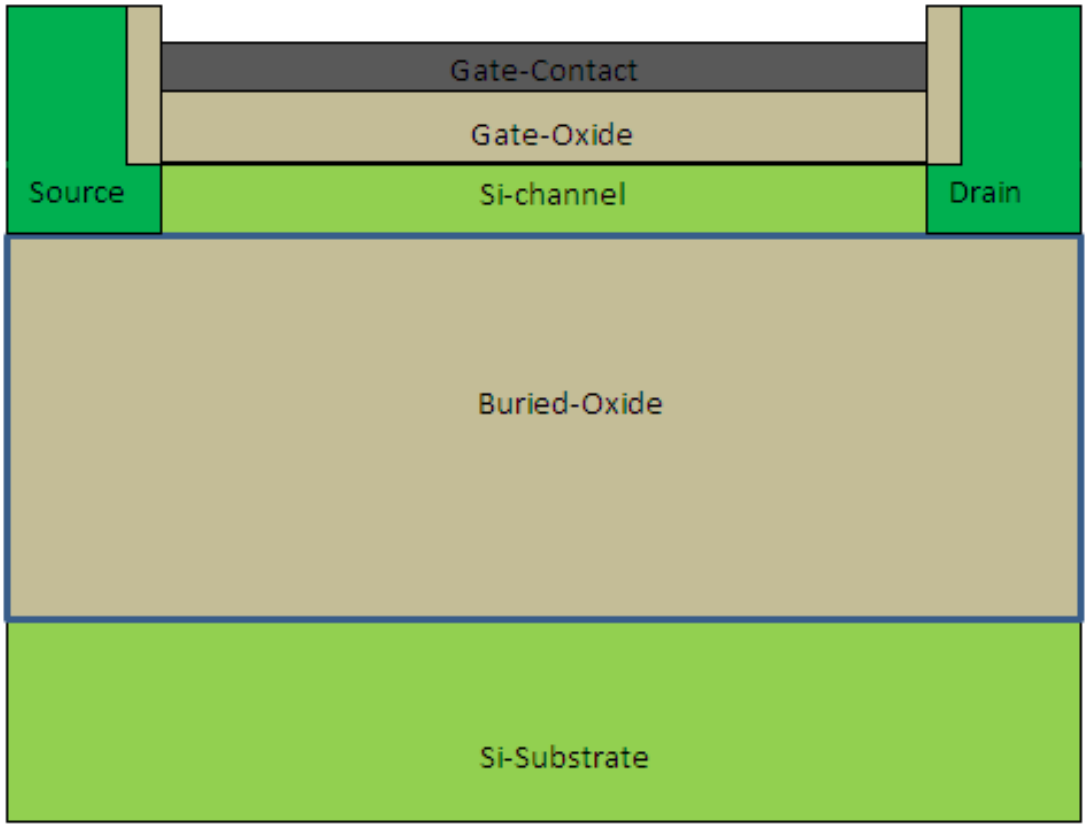

Figure 2.1: Elevated S/D SOI MOSFET

2.2 Re-S/D SOI MOSFET: Model and Simulation Literatures

Simulation based study of Re-S/D SOI MOSFETs has been presented in [33-34] [35-38] and the device structure have been compared with Raised-S/D structures with respect to parasitic capacitances, S/D contact and series resistances, SCE immunity and DIBL. Higher source/drain-to-gate coupling capacitances has been reported in [33-34] and [35] with Raised-S/D structure. The very recent work [35] has emphasized Re-S/D in SOI considering low S/D resistance at low parasitic coupling with gate electrode. The works [36-38] have reported that Raised-S/D has higher S/D series resistance than Re-S/D and upon aggressive scaling it increases rapidly along with short channel immunity degradation. The authors [37-38] have also shown that it term of

SCE immunity, Re-S/D and Raised-S/D show similar behavior however, a slight bitter DIBL has been observed in case of Re-S/D. Thus feasibility of Re-S/D structure has been defended up to 10nm [38]. On the other hand, in [39] the authors have seriously questioned the scaling of elevated S/D UTB device in sub 20-nm CMOS technology with acceptable series resistance due to some critical requirement in doping profile abruptness and spacer length.

Further, the Re-S/D structure is being applied with other technologies to improve the performance of the devices. A post-fabrication Re-S/D UTB SOI MOSFET device has been reported at 30nm channel length in [40] with good SCE immunity, little punch-through, reasonable DIBL and subthreshold slope, with heavily doped poly-silicon filled in the recessed buried oxide. In [41] Enhanced Stress Proximity technique with Re-S/D structure has been reported.

A number of literatures have been published to characterize Re-S/D SOI MOSFET in tens of nm of channel length [24-27] and [42]. In [24-25] and [42] superiority of the Re-S/D structure over the elevated-s/d structure in SOI MOSFETs have been reported. Moreover, it has been claimed that the structure could be a viable option up to 10nm technology node.

Also a number of attempts have been made to model and analyze the threshold and subthreshold characteristics for the Re-S/D SOI MOSFETs [25, 26, 27 and 43]. An threshold voltage model in analytic form has been developed for the device in [25] assuming a parabolic potential approximation in the channel. Sivilic et al. [26] have presented an analytical subthreshold slope model for the Re-S/D SOI MOSFETs again using parabolic approximation method. Following the method of [25], Saramekala et al. [27] have also presented threshold voltage model for Re-S/D SOI MOSFETs using dual-metal-gate and have reported improved hot-carrier characteristic with two metal gate in series contact. Next, Ref. [43] has developed

subthreshold current and subthreshold slope of Re-S/D SOI MOSFET using dual material gate and simulated the device to show the model accuracy. However, in all of these literatures a parabolic approximation of channel potential has been assumed and also back gate substrate induced surface potential (SISP) effect has been neglected without providing any explanation throughout range of device parameters. This negligence of the SISP effect though makes the model simple but limits the range of device parameters to be modeled accurately.

2.3 Improvement Proposed

In the present literature Poisson's equation has been solved using Evanescent mode analysis which causes improve in model accuracy. In this channel potential is broken into potential due to one-dimensional long-channel consideration and two-dimensional short-channel effective potential. Also, the inclusion of one-dimensional Poisson's equation in the substrate region is accounted to consider the effect of substrate induced surface potential (SISP) at substrate/buried-oxide interface. The inclusion of SISP effects leads to improved model accuracy for undoped or lightly doped substrate with variation of substrate voltage.

2.4 Problem Statement

The dissertation presents the study of Recessed Source/Drain Ultra-thin Body SOI MOSFET in sub-threshold region of operation in which the following parameters are modeled and explained.

a. Two-dimensional channel potential using Evanescent mode analysis

b. The dominance of front or back surface of the channel and corresponding threshold voltage

c. Device threshold voltage

d. Subthreshold characteristics of the device

e. Substrate Induced Surface Potential effects on the channel potential, threshold voltage and sub-threshold characteristics of the device.

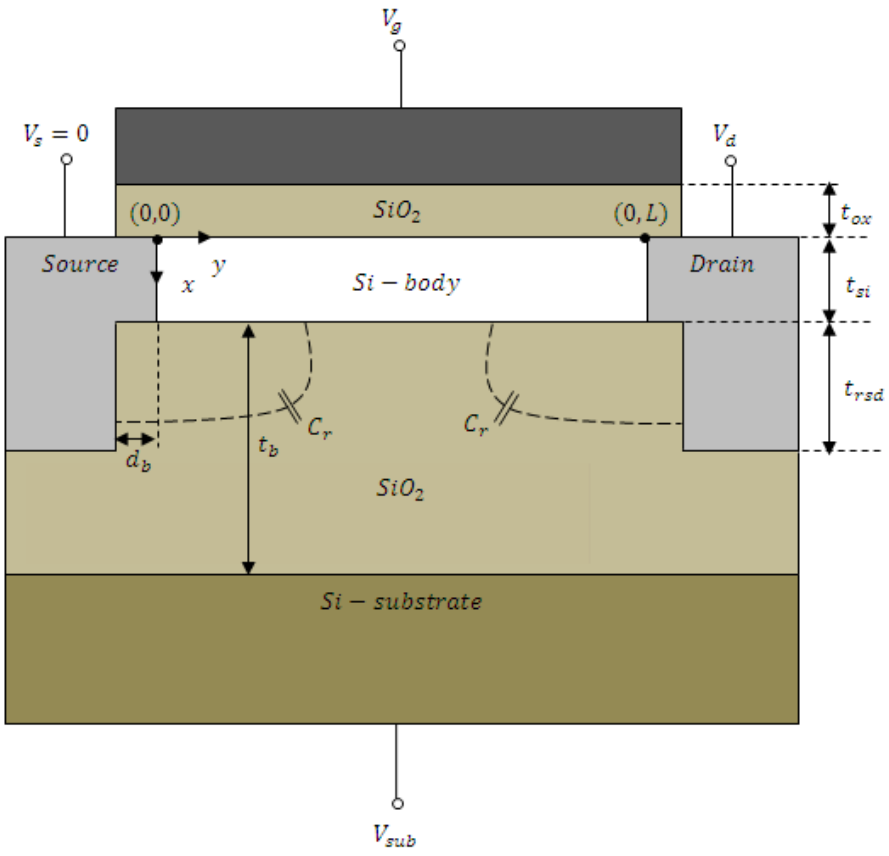

Figure 2.2: Structure of Recessed Source/Drain SOI MOSFET with the associated parameters

CHAPTER 3

TWO DIMENSIONAL SURFACE POTENTIAL MODELING

3.1 Introduction

The field effect transistor is basically a voltage controlled semiconductor device. It works with dc voltage biasing needed to create an electrostatic field or electrostatic potential between source and drain region. In SOI MOSFET the region between source and drain is called Channel or Si-body whose electrostatic potential is controlled externally using dc gate voltage. The surface potential of the channel is in general three dimensional but two dimensional potential along length and height produce enough result to analyze SOI device. The surface potential varies along channel length and thickness. However in general in SOI MOSFET the region close to the gate used to be at higher potential but in case of Re-S/D structure due to the coupling from recessed-s/d portion the channel to BOX interface area may achieve higher potential depending on recessed-s/d depth and other parameters. The modeling of surface potential is being carried out in the next sub-section and results are discussed after that. To demonstrate complete picture of surface potential SISP effect modeling has been followed by surface potential model.

3.2 Poisson's Equation and Boundary Conditions

The two-dimensional potential of channel region, $\varphi(x,y)$, in subthreshold regime of device operation is determined from following Poisson's equation

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{si}} \tag{3.1}$$

Boundary conditions for Si-body may be written as given in Equations (3.2) to (3.5) which are utilized to solve the Poisson's equation.

$$\varphi(x,0) = V_{bi} \tag{3.2}$$

$$\varphi(x,L) = V_{ds} + V_{bi} \tag{3.3}$$

$$\varepsilon_{si} \cdot \frac{\partial\varphi(x,y)}{\partial x}\Big|_{x=0} = \varepsilon_{ox} \cdot \frac{\varphi(0,y)-(V_g-V_{fb1})}{t_{ox}} \tag{3.4}$$

$$\varepsilon_{si} \cdot \frac{\partial\varphi(x,y)}{\partial x}\Big|_{x=t_{si}} = \varepsilon_b \cdot \frac{(V_d-V_{fb2})-\varphi(t_{si},y)}{t^*_{rsd}} + \varepsilon_b \cdot \frac{(V_s-V_{fb2})-\varphi(t_{si},y)}{t^*_{rsd}} + \varepsilon_b \cdot \frac{(V_{sub}-V_{fb3})+\Delta V-\varphi(t_{si},y)}{t_b} \tag{3.5}$$

where, t^*_{rsd} is a hypothetical concept called effective thickness of s/d extension in BOX, $\varphi(0,y)$ and $\varphi(t_{si},y)$ are front-surface and back-surface potentials of the channel respectively, and ΔV is substrate induced surface potential at substrate/BOX junction. The SISP effect parameter ΔV depends on substrate doping and applied bias to the substrate, as given in Section 3.4.

The capacitances associated with the device may be expressed as below

$$C_{si} = \frac{\varepsilon_{si}}{t_{si}} \tag{3.6}$$

$$C_b = \frac{\varepsilon_b}{t_b} \tag{3.7}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.8}$$

$$C_r = \frac{\varepsilon_b}{t^*_{rsd}} \tag{3.9}$$

where all the symbols are explained in the List of Symbols section. However C_r may be calculated as done in [25] for low drain voltage assuming equal coupling to the back surface of channel from recessed source and drain side. The expression is given below in Eq. (3.10).

$$C_r = \begin{cases} \frac{\varepsilon_b}{\frac{\pi}{2}\left(1+sech\frac{\mathrm{t_{rsd}}}{\mathrm{d_b}}\right)} \cdot ln\left(1+\frac{L}{2d_b}\right) & \text{for } \frac{L}{2} < t_{rsd} \\ \frac{\varepsilon_b}{\frac{\pi}{2}\left(1+sech\frac{\mathrm{t_{rsd}}}{\mathrm{d_b}}\right)} \cdot ln\left(1+\frac{t_{rsd}}{d_b}\right) & \text{for } \frac{\mathrm{L}}{2} > \mathrm{t_{rsd}} \text{ or } \mathrm{t_{rsd}} = 0 \end{cases} \quad (3.10)$$

3.3 Generalized 2-D Channel Potential

The 2D potential $\varphi(x,y)$ is decoupled as follows

$$\varphi(x,y) = V(x) + U(x,y) \quad (3.11)$$

where $V(x)$ is long-channel potential, and $U(x,y)$ is short-channel effect in channel potential. Thus Equation (3.1) may be expressed as combination of Equations (3.12) and (3.13) as

$$\frac{\partial^2 V(x)}{\partial x^2} = \frac{qN_a}{\varepsilon_{si}} \quad (3.12)$$

$$\frac{\partial^2 U(x,y)}{\partial x^2} + \frac{\partial^2 U(x,y)}{\partial y^2} = 0 \quad (3.13)$$

Upon integrating Eq. (3.12) a generalized 1D potential along x-axis may be obtained as

$$V(x) = \frac{qN_a}{\varepsilon_{si}} \cdot x^2 + \left(\frac{V_{sb}-V_{sf}}{t_{si}} - \frac{qN_a t_{si}}{\varepsilon_{si}}\right) \cdot x + V_{sf} \quad (3.14)$$

where V_{sf}, and V_{sb} are long-channel front and back surface potential which may obtained using boundary conditions (3.4) and (3.5). The expressions for V_{sf}, and $V_{sb}$are given below

$$V_{sf} = \frac{C_{ox}(2C_r+C_b+C_{si})}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)}\left(V_g - V_{fb1}\right) - \frac{C_{ox}C_{si}}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)} \cdot \left[\frac{qN_a t_{si}}{C_{ox}}\left(1+\frac{2C_r+C_b}{2C_{si}}\right) - \frac{C_r}{C_{ox}}\left(V_d+V_s-2V_{fb2}\right) - \frac{C_b}{C_{ox}}\left(V_{sub}-V_{fb3}+\Delta V\right)\right] \quad (3.15)$$

$$V_{sb} = \frac{C_{si}C_{ox}}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)}\left(V_g - V_{fb1}\right) - \frac{C_{si}(C_{si}+C_{ox})}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)} \cdot \left[\frac{qN_a t_{si}}{2C_{si}}\left(\frac{2C_{si}+C_{ox}}{C_{si}+C_{ox}}\right) - \frac{C_r}{C_{si}}\left(V_d+V_s-2V_{fb2}\right) - \frac{C_b}{C_{si}}\left(V_{sub}-V_{fb3}+\Delta V\right)\right] \quad (3.16)$$

Method of variable separation is used to solve Eq. (3.13) with boundary conditions of Eqs. (3.2) to (3.5) in order to determine following series solution of short-channel front surface potentials, $U(0,y)$, and back surface potentials, $U(t_{si},y)$,

$$U(0,y)=\sum_{n=1}^{\infty}\frac{(V_{ds}+V_{bi}-V_{sf})\sinh(\lambda_n y)+(V_{bi}-V_{sf})\sinh(\lambda_n(L-y))}{\sinh(\lambda_n L)} \tag{3.17}$$

and

$$U(t_{si},y)=\sum_{n=1}^{\infty}\frac{(V_{ds}+V_{bi}-V_{sb})\sinh(\lambda_n y)+(V_{bi}-V_{sb})\sinh(\lambda_n(L-y))}{\sinh(\lambda_n L)} \tag{3.18}$$

where, the parameter λ_n is associated with channel and called inverse characteristic length given as

$$\lambda_n t_{si}=\frac{C_{si}}{C_b+C_{ox}+2C_r}\left[(\lambda_n t_{si})^2-\frac{C_{ox}C_b+2C_{ox}C_r}{{C_{si}}^2}\right]\tan(\lambda_n t_{si}) \tag{3.19}$$

Out of infinite numbers of solutions of λ_n in Equations (3.17) and (3.18) only lowest-order solution (λ_1) is significant near to the point of our interest ($y=\frac{L}{2}$) owing to the sine hyperbolic function [44]. Assuming the desired root to be $\lambda_1=\lambda$, the modified equations may be given as follows

$$U(0,y)=\frac{(V_{ds}+V_{bi}-V_{sf})\sinh(\lambda y)+(V_{bi}-V_{sf})\sinh(\lambda(L-y))}{\sinh(\lambda L)} \tag{3.20}$$

$$U(t_{si},y)=\frac{(V_{ds}+V_{bi}-V_{sb})\sinh(\lambda y)+(V_{bi}-V_{sb})\sinh(\lambda(L-y))}{\sinh(\lambda L)} \tag{3.21}$$

$$\lambda t_{si}=\frac{C_{si}}{C_b+C_{ox}+2C_r}\left[(\lambda t_{si})^2-\frac{C_{ox}C_b+2C_{ox}C_r}{{C_{si}}^2}\right]\tan(\lambda t_{si}) \tag{3.22}$$

Thus, the front and back channel surface potentials $\varphi(0,y)$ and $\varphi(t_{si},y)$ respectively of short-channel Re-S/D SOI MOSFETs are obtained by using Equations (3.20) and (3.21) into Eq. (3.11) respectively as

$$\varphi(0,y)=V_{sf}+\frac{(V_{ds}+V_{bi}-V_{sf})\sinh(\lambda y)+(V_{bi}-V_{sf})\sinh(\lambda(L-y))}{\sinh(\lambda L)} \tag{3.23}$$

and

$$\varphi(t_{si},y) = V_{sb} + \frac{(V_{ds}+V_{bi}-V_{sb})\sinh(\lambda y)+(V_{bi}-V_{sb})\sinh(\lambda(L-y))}{\sinh(\lambda L)} \quad (3.24)$$

The Equations (3.23) and (3.24) represents front surface potential and back surface potential of the channel. However the generalized surface potential may be obtained as generalized solution of Eq. (3.13) as given below

$$U(x,y) = [\cos(\lambda x) + P \cdot sin(\lambda x)]\left[Q \cdot e^{\lambda y} + R \cdot e^{-\lambda y}\right] \quad (3.25)$$

where

$$P = \frac{1}{\lambda t_{si}} \cdot \frac{C_{ox}}{C_{si}} \quad (3.26)$$

$$Q = \frac{[V_{ds}+V_{bi}-V(x)]-[V_{bi}-V(x)]\mathrm{e}^{-\lambda L}}{[cos(\lambda L)+P\cdot\sin(\lambda L)]\left[\mathrm{e}^{\lambda L}-\mathrm{e}^{-\lambda L}\right]} \quad (3.27)$$

$$R = \frac{[V_{bi}-V(x)]\mathrm{e}^{\lambda L}-[V_{ds}+V_{bi}-V(x)]}{[cos(\lambda L)+P\cdot\sin(\lambda L)]\left[\mathrm{e}^{\lambda L}-\mathrm{e}^{-\lambda L}\right]} \quad (3.28)$$

and λ is same as given in Eq. (3.22). Thus substituting $V(x)$ and $U(x,y)$ from Eqs. (3.13) and (3.25) respectively into Eq. (3.11) the complete 2D channel potential in generalized form may be obtained as

$$\varphi(x,y) = \frac{qN_a}{\varepsilon_{si}} \cdot x^2 + \left(\frac{V_{sb}-V_{sf}}{t_{si}} - \frac{qN_a t_{si}}{\varepsilon_{si}}\right) \cdot x + V_{sf} + [\cos(\lambda x) + P \cdot sin(\lambda x)]\left[Q \cdot e^{\lambda y} + R \cdot e^{-\lambda y}\right] \quad (3.29)$$

It is to note that to find the threshold voltage Equations (3.23) and (3.24) are sufficient since the front or back surface dominance potential is considered. However for subthreshold analysis generalized potential is a necessary equation which will be carried out in Chapter 5 while modeling current in subthreshold region of operation.

3.4 Model of Substrate Induced Surface Potential

The electrostatic potential difference between the substrate/box interface and neutral substrate region is accounted as Substrate Induced Surface Potential (SISP), i.e., $\Delta V = \Psi_{s3} - \Psi_{sub}$, where Ψ_{s3} and $\Psi_{sub}(= V_{sub} - \Phi_{Fsub})$ are potentials at substrate/box interface and neutral substrate region, respectively [45]. Poisson's equation given below has been solved in the substrate region to obtain SISP effect.

$$\frac{\partial^2 \Psi}{\partial x^2} = \frac{q}{\varepsilon_{si}}\left(N_{sub} + n_o e^{\frac{q\Psi(x)}{KT}} - p_o e^{\frac{-q\Psi(x)}{KT}}\right) \tag{3.30}$$

where, $\Psi(x)$ is potential distribution in the substrate region, while

$$n_o = \frac{{n_i}^2}{N_{sub}} e^{\frac{-q\left(V_{sub}-V_{fb3}\right)}{KT}} \tag{3.31}$$

and

$$p_o = N_{sub} e^{\frac{q\left(V_{sub}-V_{fb3}\right)}{KT}} \tag{3.32}$$

are electrons and holes concentrations in the substrate region due to applied substrate bias voltage. Where the symbols are taken as per the List of Symbols defined early in the work. Equation (3.30) has been solved to get the electric field, E_{s3}, at BOX-substrate interface.

$$E_{s3} = \sqrt{\frac{2q}{\varepsilon_{si}}\left[N_{sub}(\Psi_{s3} - \Psi_{sub}) + \frac{kT}{q} n_o \left(e^{\frac{q\Psi_{s3}}{KT}} - e^{\frac{q\Psi_{sub}}{KT}}\right) + \frac{kT}{q} p_o \left(e^{\frac{-q\Psi_{s3}}{KT}} - e^{\frac{-q\Psi_{sub}}{KT}}\right)\right]} \tag{3.33}$$

Now, electric field at front surface of silicon body, E_{s1} , and electric field at back surface of silicon body, E_{s2} , may be related as [45]

$$E_{s2} = E_{s1} - \frac{qN_a}{C_{si}} \tag{3.34}$$

Similarly, E_{s2} may also be related with E_{s3} , as follows

$$E_{s3} = E_{s2} + \frac{\varepsilon_b}{\varepsilon_{si}} \frac{(V_d - V_{fb2}) - V_{sb}}{t^*_{rsd}} + \frac{\varepsilon_b}{\varepsilon_{si}} \frac{(V_s - V_{fb2}) - V_{sb}}{t^*_{rsd}} \tag{3.35}$$

Upon substitution of Eqs. (3.34) and (3.35) into Eq. (3.33) the result is obtained as

$$V_g - V_{fb1} = V_{sft} + \frac{qN_a t_{si}}{C_{ox}} - \frac{C_r}{C_{ox}}\left(V_d + V_s - 2V_{fb2}\right) + \frac{2C_r}{C_{ox}}V_{sbt} + \frac{C_{si}}{C_{ox}}f(\Delta V) \tag{3.36}$$

where,

$$f(\Delta V) = \left[\frac{2qt_{si}N_{sub}}{C_{si}}\left\{\Delta V + \frac{KT}{q}\left(\frac{n_i}{N_{sub}}\right)^2\left(e^{\frac{q\Delta V}{KT}} - 1\right) + \frac{KT}{q}\left(e^{\frac{-q\Delta V}{KT}} - 1\right)\right\}\right]^{1/2} \tag{3.37}$$

Eventually, Eq. (3.15) is utilized in Eq. (3.36) to obtain

$$\Delta V = \left(\frac{2C_r+C_b}{C_b}\right)V_{sft} - \left(\frac{C_r}{C_{si}}\right)\left(\frac{2C_r+C_b+C_{si}}{C_b}\right)2V_{sbt} - \left(\frac{2C_r+C_b}{2C_b}\right)\frac{qN_a t_{si}}{C_{si}} - V_{sub} + V_{fb3} +$$

$$\left(\frac{C_r}{C_{si}}\right)\left(\frac{2C_r+C_b}{C_b}\right)\left(V_d + V_s - 2V_{fb2}\right) - \left(\frac{2C_r+C_b+C_{si}}{C_b}\right)f(\Delta V) \tag{3.38}$$

Thus, ΔV of Eq. (33) accounts the effect of SISP in the present model, and it reduces to Eq. (10) of [44] when $C_r = 0$ is substituted. It has been utilized throughout the work in all cases of surface potential, threshold voltages, and sub-threshold characteristics of the Re-s/d SOI MOSFET.

3.5 Result and Discussion

This sub section being with Figure 3.1 which depicts the variation of SISP effects with respect to the applied substrate bias. The variation of ΔV can be observed from the plot of SISP effect versus substrate voltage. As ΔV varies between zero in accumulation region to $2\frac{kT}{q}ln\frac{N_{sub}}{n_i}$ in inversion region depending upon applied substrate voltage with device parameters being constant. SISP effect has been solved from Eq. (3.38) within the extreme limits of the ΔV variation. The solution of Eq. (3.38) has been obtained numerically using MATLAB.

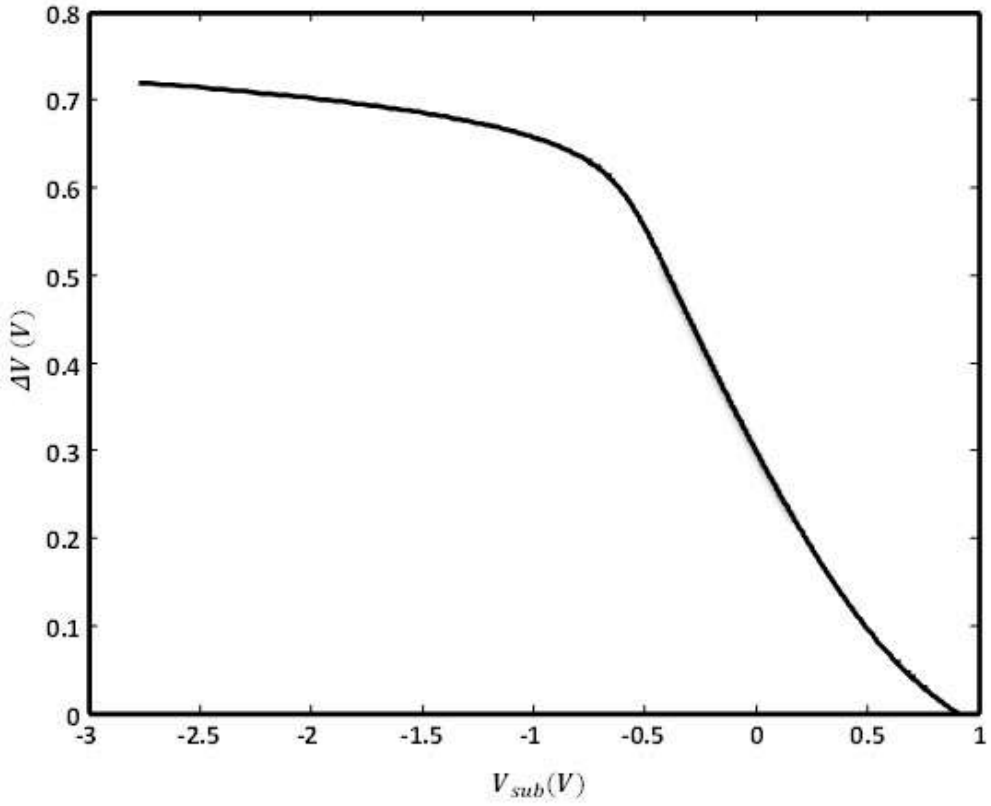

Figure 3.1: Variation of ΔV versus substrate voltage (V_{sub}) at $L = 60nm$, $t_{ox} = 2nm$, $t_{si} = 5nm$, $t_{rsd} = 30nm$, $t_b = 200nm$, $N_a = N_{asub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, and $V_d = 0.1V$.

Next, the front and back surface potential obtained from Equations (3.23) and (3.24) has been plotted in Figs. 3.2 and 3.3. Figure 3.2 shows the front and back surface potential of channel in the direction of channel length for the device parameters and bias voltages depicted in the figure caption. Clearly the minimum value of back surface potential is larger than that of front surface potential and hence back surface dominant the conduction. It must be noted that the observation is for channel doping of $10^{15}cm^{-3}$. The plot of back surface potential with variation in t_{rsd} is shown in Fig 3.3 to observe the effect of recessed source/drain portion. As shown with increase in recessed depth the minimum potential increases up to particular t_{rsd} and thereafter

saturates owing to maximum coupling. Thus it can be said that addition of recessed-s/d structure takes participation in the potential profile and mostly it causes back surface of the channel to be increase significantly.

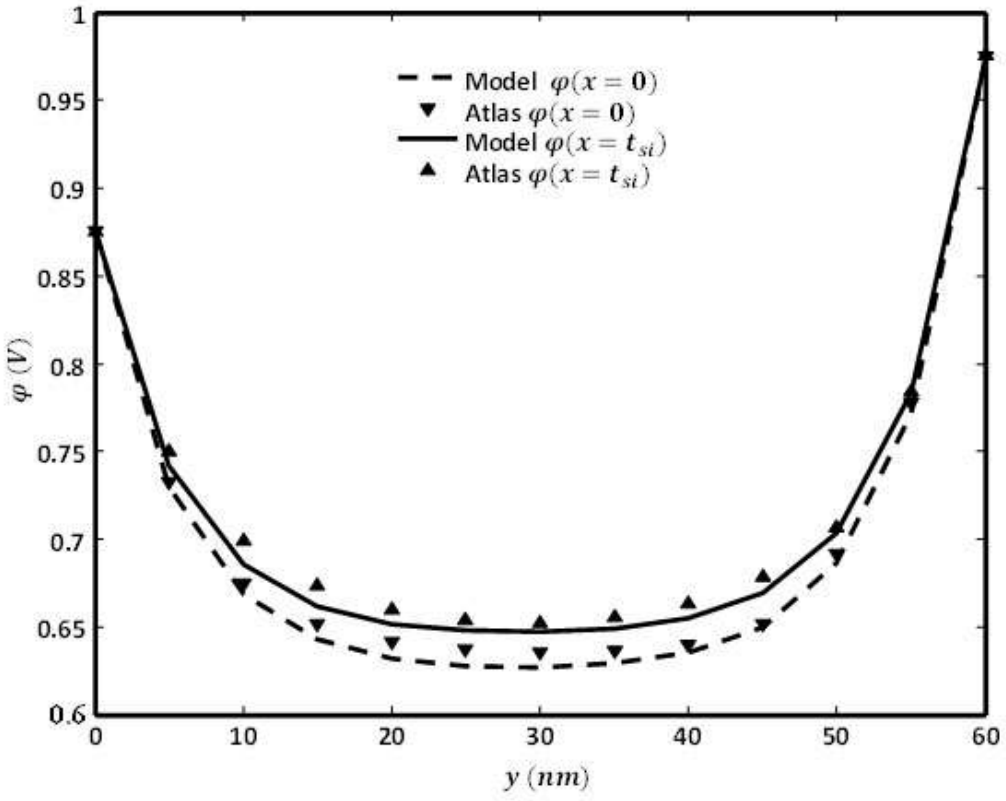

Figure 3.2: Surface potential (φ) curve in the direction of channel length (y) at $L = 60nm$, $t_{ox} = 2nm$, $t_{si} = 5nm$, $t_{rsd} = 30nm$, $t_b = 200nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_g = 0.4V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

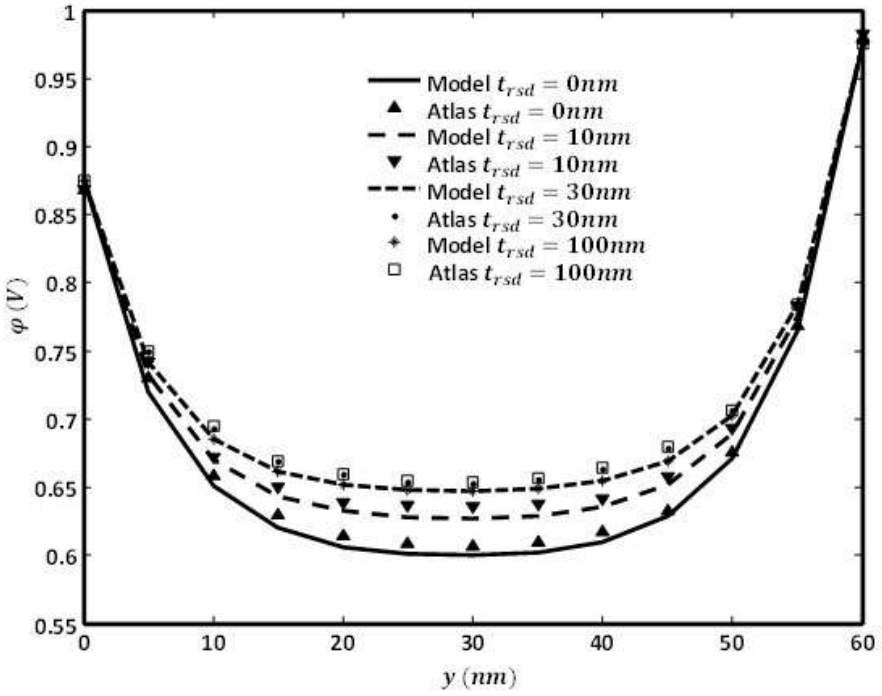

Figure 3.3: Back-surface potential ($\varphi|_{x=t_{si}}$) curve in the direction of channel length (y) at $L = 60nm$, $t_{ox} = 2nm$, $t_{si} = 5nm$, $t_b = 200nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_{ox} = 0.4V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

CHAPTER 4

THRESHOLD VOLTAGE OF THE DEVICE

3.1 Introduction

The MOSFETs being used as switch need an external control which can define the on and off nature. DC voltage is used as the external control in MOSFET device and hence may be called as voltage controlled device. This dc voltage needed to switch on the MOSFET is called threshold voltage at which a reasonable drain current is achieved.

In the language of physics, it is the voltage at which the channel gets inverted and depends on the device dimensions and materials utilized while manufacturing [25], [33] and [45]. The same definition of physics is being applied here to find the threshold voltage expression in sub section 4.2. Obviously, threshold voltage will depend on device dimensions and parameters chosen and thus the variation in threshold voltage is being studied in the next sub section 4.3.

4.2 Device Threshold Voltage

The threshold voltage of a FD SOI MOSFET with highly doped channel could be characterized as the applied gate voltage at which minimum of the surface potential becomes $2\Phi_F$ [25], where Φ_F is the Fermi potential of the channel region. However, considering generalized case for channel doping the following definition of threshold voltage has been applied for the recessed device in this work [45].

$$\varphi(x=0/t_{si},y)|_{min}|_{V_g=V_{thf}/V_{thb}} = 2\Phi_F^* = \begin{cases} 2\Phi_F & for,\ N_a > n_T \\ \Phi_F + \frac{kT}{q}\ln\left(\frac{n_T}{n_i}\right) & for,\ N_a < n_T \end{cases} \quad (4.1)$$

where, V_{thf}, and V_{thb} are front surface controlled threshold voltages and back surface controlled threshold voltage respectively. And n_T is a critical concentration of electron in channel to turn on the device [46-47]. The parameter n_T depends on device parameters which has been determined following the method of Chen et al. [47].

The front surface minimum potential is obtained from Eq. (3.23) as

$$\varphi(x=0,y)|_{min} = V_{sf} + 2\cdot\sqrt{\alpha\beta}\cdot e^{-\lambda L/2} \quad (4.2)$$

where,

$$\alpha = \frac{[(V_{bi}-V_{sf})-(V_{ds}+V_{bi}-V_{sf})e^{-\lambda L}]}{1-e^{-2\lambda L}} \quad (4.3)$$

$$\beta = \frac{[(V_{ds}+V_{bi}-V_{sf})-(V_{bi}-V_{sf})e^{-\lambda L}]}{1-e^{-2\lambda L}} \quad (4.4)$$

and back surface minimum potential is obtained from Eq. (3.24) as

$$\varphi(x=t_{si},y)|_{min} = V_{sb} + 2\cdot\sqrt{\alpha'\beta'}\cdot e^{-\lambda L/2} \quad (4.5)$$

where,

$$\alpha' = \frac{[(V_{bi}-V_{sb})-(V_{ds}+V_{bi}-V_{sb})e^{-\lambda L}]}{1-e^{-2\lambda L}} \quad (4.6)$$

$$\beta' = \frac{[(V_{ds}+V_{bi}-V_{sb})-(V_{bi}-V_{sb})e^{-\lambda L}]}{1-e^{-2\lambda L}} \quad (4.7)$$

Using Eq. (4.2) into Eq. (4.1), we get the following expression

$$V_{sft} + 2\cdot\sqrt{\alpha\beta}\cdot e^{-\lambda L/2} = 2\Phi_F^* \quad (4.8)$$

where,

$$V_{sft} = V_{sf}\big|_{V_g=V_{thf}} \quad (4.9)$$

Further Eq. (4.8) can be simplified as explicit equation as given below by second order polynomial.

$$A_1 \cdot {V_{sft}}^2 + A_2 \cdot V_{sft} + A_3 = 0 \tag{4.10}$$

where,

$$A_1 = 4e^{-\lambda L}\left(1 - e^{-\lambda L}\right)^2 - \left(1 - e^{-2\lambda L}\right)^2 \tag{4.11}$$

$$A_2 = 4\Phi_F^*\left(1 - e^{-2\lambda L}\right)^2 - 4(V_{ds} + 2V_{bi})e^{-\lambda L}\left(1 - e^{-\lambda L}\right)^2 \tag{4.12}$$

$$A_3 = 4V_{bi}(V_{ds} + V_{bi})\left(e^{-\lambda L}\right)\left(1 + e^{-2\lambda L}\right) - 4\{(V_{bi})^2 + (V_{ds} + V_{bi})^2\}e^{-2\lambda L}$$

$$-4{\Phi_F^*}^2\left(1 - e^{-2\lambda L}\right)^2 \tag{4.13}$$

Eq. (4.10) is a quadratic equation and its root could be easily obtained as

$$V_{sft} = \frac{-A_2 + \sqrt{{A_2}^2 - 4A_1A_3}}{2A_1} \tag{4.14}$$

Now, at threshold condition ($V_g = V_{thf}$), V_{sf}becomes V_{sft} and hence Eq. (3.15) could be modified as

$$V_{sft} = \frac{C_{ox}(2C_r + C_b + C_{si})}{C_{ox}C_{si} + (C_{si} + C_{ox})(2C_r + C_b)}\left(V_{thf} - V_{fb1}\right) - \frac{C_{ox}C_{si}}{C_{ox}C_{si} + (C_{si} + C_{ox})(2C_r + C_b)} \cdot$$

$$\left[\frac{qN_at_{si}}{C_{ox}}\left(1 + \frac{2C_r + C_b}{2C_{si}}\right) - \frac{C_r}{C_{ox}}\left(V_d + V_s - 2V_{fb2}\right) - \frac{C_b}{C_{ox}}\left(V_{sub} - V_{fb3} + \Delta V\right)\right] \tag{4.15}$$

After rearranging the terms of Eq. (4.15), following equation of front channel threshold voltage, V_{thf}, could be obtained

$$V_{thf} = V_{fb1} + V_{sft} \cdot \frac{C_{si}}{2C_r + C_b + C_{si}} \cdot \left[1 + \left(\frac{C_{si} + C_{ox}}{C_{ox}}\right)\left(\frac{2C_r + C_b}{C_{si}}\right)\right] + \frac{C_{si}}{2C_r + C_b + C_{si}} \cdot$$

$$\left[\frac{qN_at_{si}}{C_{ox}}\left(1 + \frac{2C_r + C_b}{2C_{si}}\right) - \frac{C_r}{C_{ox}}\left(V_d + V_s - 2V_{fb2}\right) - \frac{C_b}{C_{ox}}\left(V_{sub} - V_{fb3} + \Delta V\right)\right] \tag{4.16}$$

Similarly, threshold voltage for back surface is given by

$$V_{thb} = V_{fb1} + V_{sbt} \cdot \frac{C_{si}+C_{ox}}{C_{ox}} \cdot \left[\left(\frac{C_{ox}}{C_{si}+C_{ox}}\right) + \left(\frac{2C_r+C_b}{C_{si}}\right)\right] + \frac{C_{si}+C_{ox}}{C_{ox}} \cdot$$

$$\left[\frac{qN_a t_{si}}{2C_{si}}\left(\frac{2C_{si}+C_{ox}}{C_{si}+C_{ox}}\right) - \frac{C_r}{C_{si}}\left(V_d + V_s - 2V_{fb2}\right) - \frac{C_b}{C_{si}}\left(V_{sub} - V_{fb3} + \Delta V\right)\right] \quad (4.17)$$

where, $V_{sbt} = V_{sb}|_{V_g=V_{thb}}$ is found from quadratic equation given below.

$$A_1 \cdot {V_{sbt}}^2 + A_2 \cdot V_{sbt} + A_3 = 0 \quad (4.18)$$

Since V_{thf} and V_{thb} are two threshold voltage model but actually the physical device becomes on if sufficient current can flow through either front or back surface of channel. The surface with higher potential will start conducting first and will ensure the threshold of physical Re-S/D SOI MOSFET. Accordingly the threshold voltage V_{th} of a recessed source/drain SOI MOSFET could be determined either by front surface threshold voltage or by the back surface threshold voltage as follows [25]

$$V_{th} = \begin{cases} V_{thf} & for,\ \varphi(x=0,y)|_{min} > \varphi(x=t_{si},y)|_{min} \\ V_{thb} & for,\ \varphi(x=0,y)|_{min} < \varphi(x=t_{si},y)|_{min} \end{cases} \quad (4.19)$$

4.3 Result and Discussion

The threshold voltage of front and back surface being formulated in Eq. (4.16) and Eq. (4.17) respectively now the comparison and discussion can be carried out with their plots with respect to threshold voltage obtained using device simulator. In Fig. 4.1 the variation of both front and back channel threshold voltages against the channel length with a channel doping of $N_a = 10^{15}\text{cm}^{-3}$ is shown. Since only back channel threshold voltage is in perfect match with the ATLAS simulation results, it can be attributed to the higher minimum of back surface potential compare to the front surface potential at such a low channel doping. Further in Figs. 4.2 and 4.3

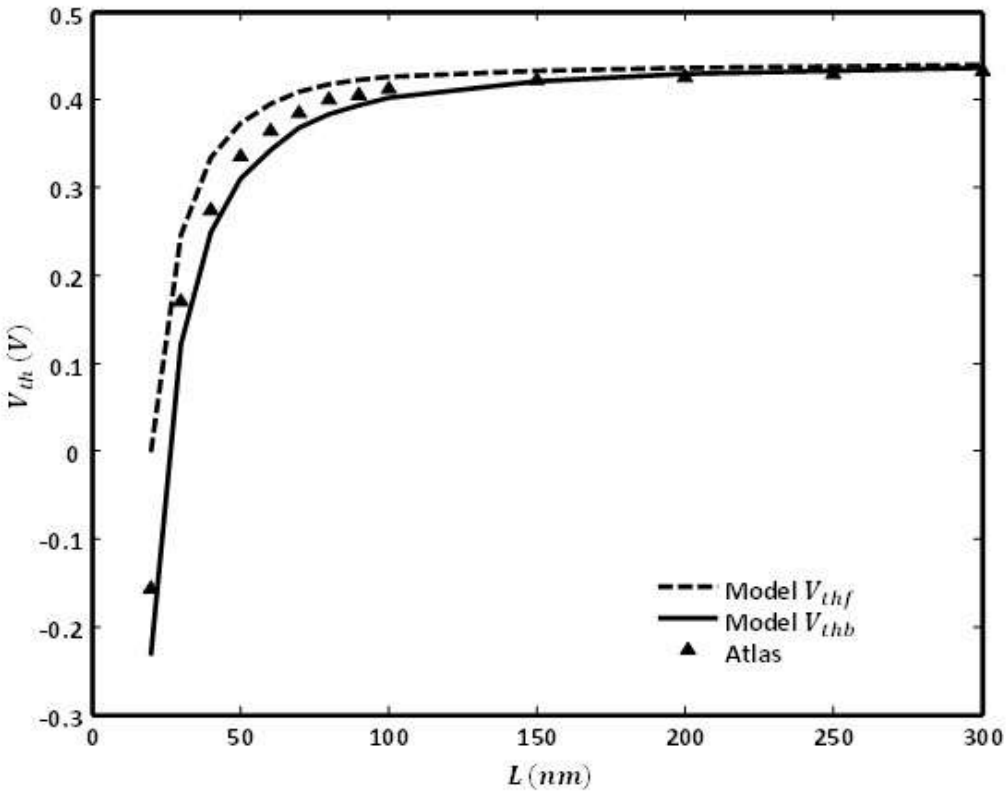

Figure 4.1: Front/ back channel threshold voltage ($V_{thf/thb}$) vs. channel length (L) at $N_a = 10^{15}\text{cm}^{-3}$, $t_{ox} = 2nm$, $t_{si} = 10nm$, $t_{rsd} = 30nm$, $t_b = 200nm$, $N_{asub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

the same kind of plots are obtained at channel doping of $N_a = 10^{17}\text{cm}^{-3}$ and $N_a = 10^{18}\text{cm}^{-3}$ respectively. Figure 4.2 shows back surface controlled inversion at $L < 100nm$ while front surface controlled inversion at higher channel length. Further fig. 4.3 shows a front surface controlled inversion of channel up to $40nm$ channel length. Match of Atlas simulation result on front and back surface potential of channel can easily be understood from Figs 4.1, 4.2 and 4.3 with the effect of channel doping. The device threshold voltage is governed by back surface

threshold voltage at low doping but as doping increase front surface dominance takes place due to improvement of gate control over channel. Thus the above result may be summarized as the switching of dominance from back surface to front surface with increase in channel doping. And now onward the device threshold voltage is plotted with front surface threshold voltage at $N_a = 10^{15}\text{cm}^{-3}$ and back surface threshold voltage at $N_a = 10^{18}\text{cm}^{-3}$ unless and until stated otherwise.

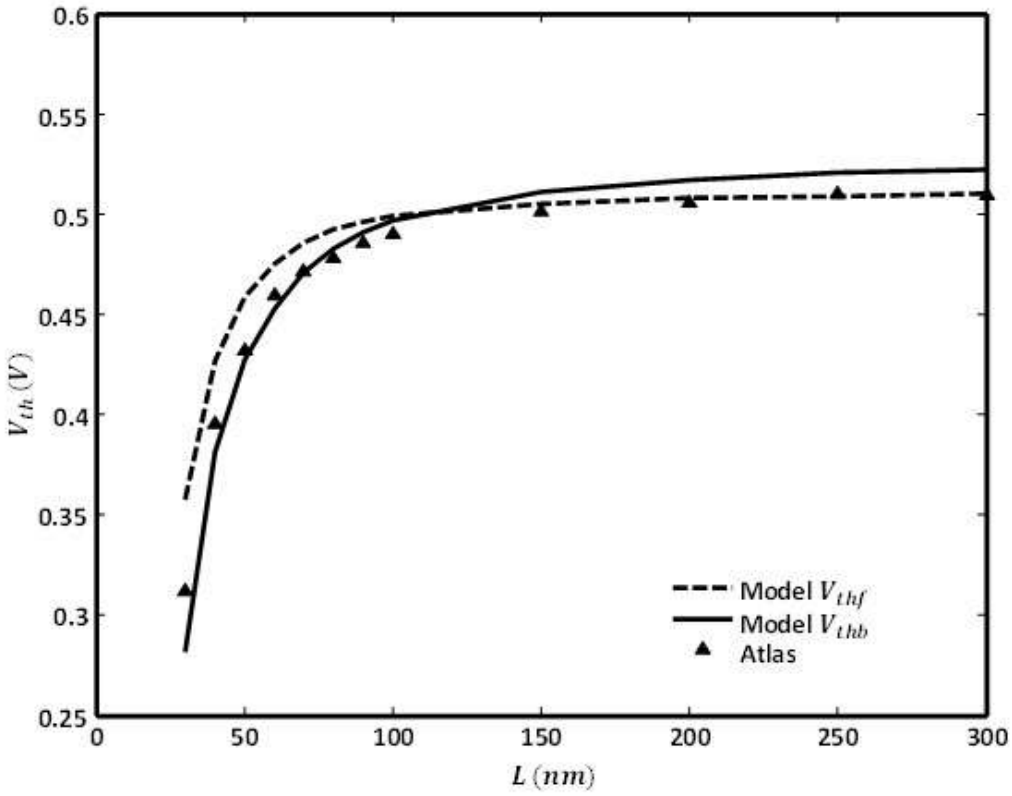

Figure 4.2: Front/ back channel threshold voltage ($V_{thf/thb}$) vs. channel length (L) at $N_a = 10^{15}\text{cm}^{-3}$, $t_{ox} = 2nm$, $t_{si} = 10nm$, $t_{rsd} = 30nm$, $t_b = 200nm$, $N_{asub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

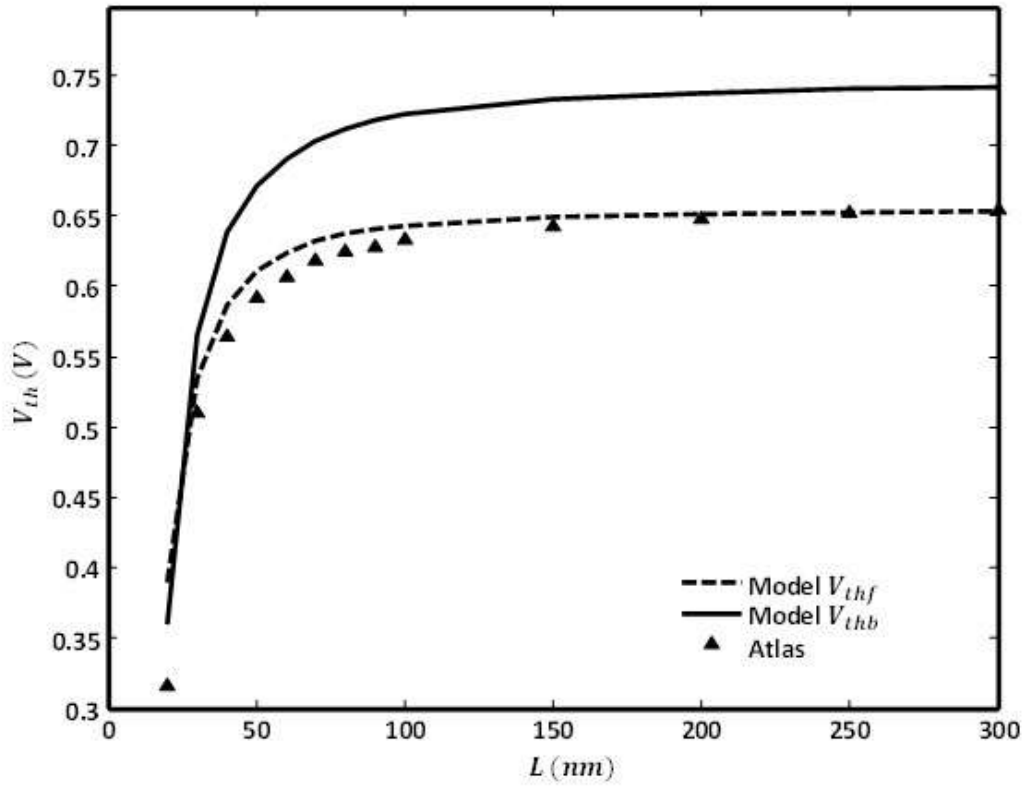

Figure 4.3: Front/ back channel threshold voltage ($V_{thf/thb}$) vs. channel length (L) at $N_a = 10^{18}\text{cm}^{-3}$, but other parameters same as Fig. 5.1

Threshold voltage variation vs. channel length for two different channel thickness is shown in Fig. 4.4 and Fig 4.5 at $N_a = 10^{15}\text{cm}^{-3}$ and $N_a = 10^{18}\text{cm}^{-3}$ respectively. The modeling result for back surface threshold voltage is being utilized in Fig. 4.4 while that of Fig. 4.5 follows front surface threshold voltage. In both the cases the roll-off increases at higher channel thickness due to loss of gate control. Thus thinner channel provide better control on short channel effects. Due to this reason with device dimension being reduced drastically the channel thickness is being scaled proportionally. This proportional scaling of channel thickness

suppresses high drain current in subthreshold region arisen due to loss of gate control in nanoscale SOI MOSFETs.

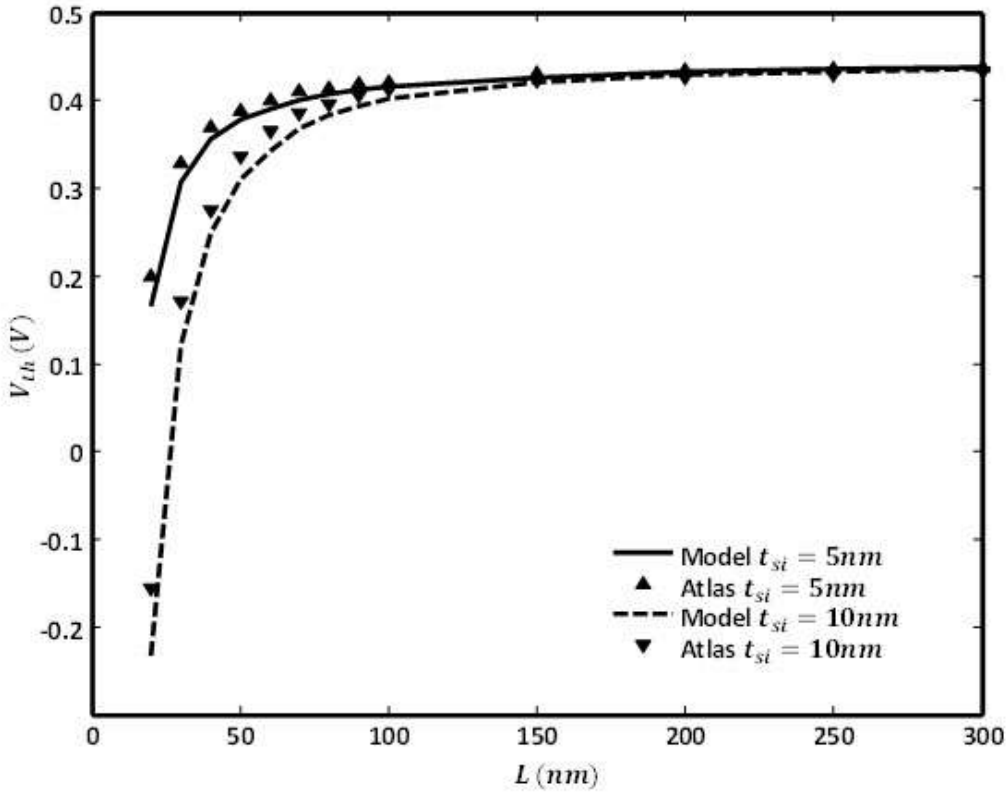

Figure 4.4: Threshold voltage (V_{th}) vs. channel length (L) for $t_{si} = 5nm$ and $10nm$ at $N_a = 10^{15}\text{cm}^{-3}$, $t_{ox} = 2nm$, $t_{rsd} = 30nm$, $t_b = 200nm$, $N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

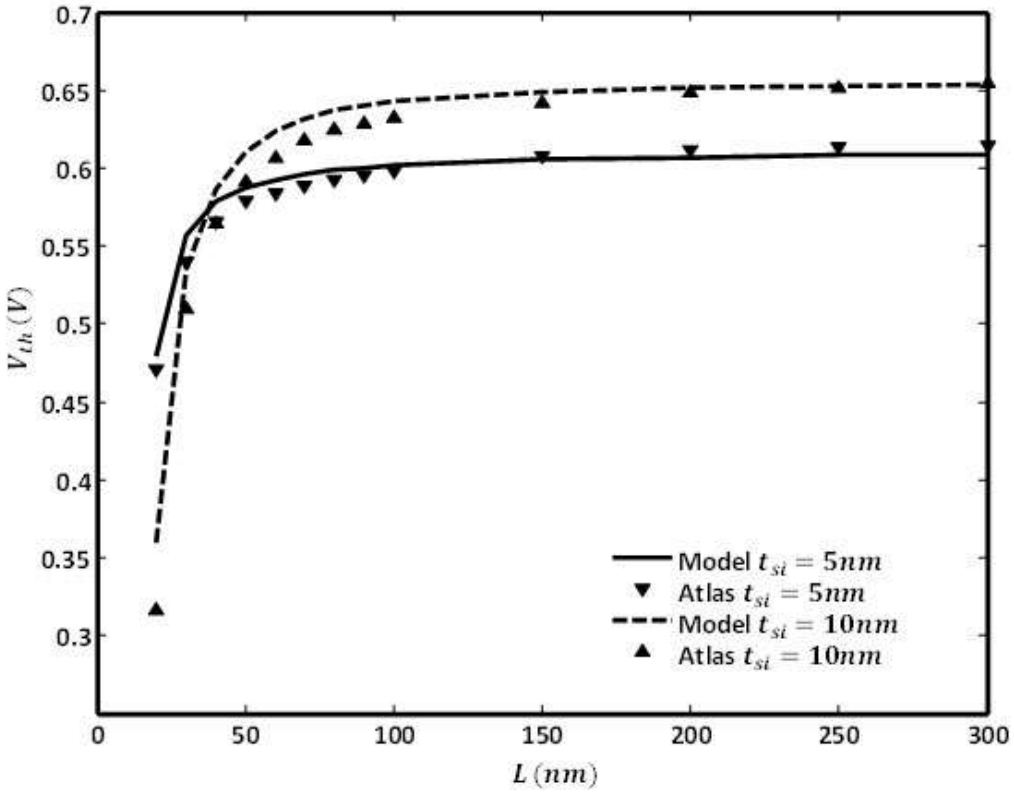

Figure 4.5: Threshold voltage (V_{th}) vs. channel length (L) for $t_{si} = 5nm$ and $10nm$ at $N_a = 10^{18}\text{cm}^{-3}$, $t_{ox} = 2nm$, $t_{rsd} = 30nm$, $t_b = 200nm$, $N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

Next the effect of gate-oxide thickness is studied in Fig. 4.6. The plot shows threshold voltage roll-off at $N_a = 10^{15}\text{cm}^{-3}$ and other parameters as given in the caption. As expected with higher gate-oxide thickness the short channel immunity decrease and thus lesser t_{ox} is better option for nanoscale SOI MOSFET.

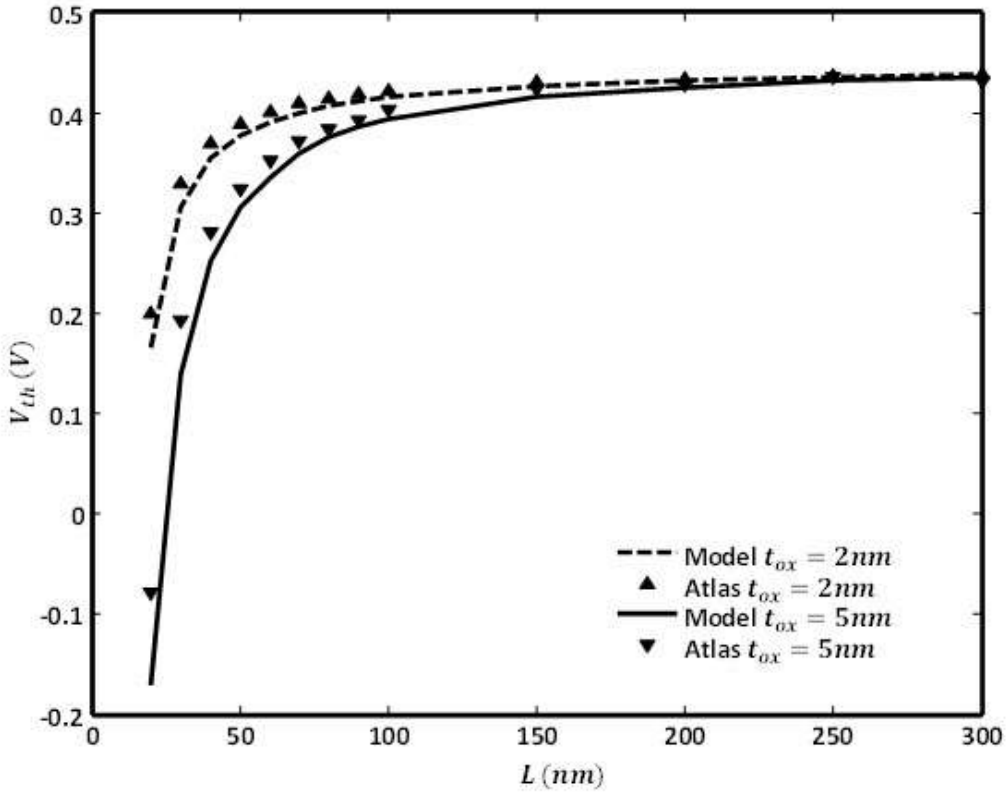

Figure 4.6: Threshold voltage (V_{th}) vs. channel length (L) at $t_{ox} = 2nm$ and $5nm$. Rest of the parameters are $t_{si} = 5nm$, $t_{rsd} = 30nm$, $t_b = 200nm$, $N_a = N_{asub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$

Figures 4.7 and 4.8 demonstrate the effect of recessed-source/drain depth in BOX. To study the recessed S/D SOI MOSFET with respect to SOI MOSFET $t_{rsd} = 0nm, 30nm$ and $100nm$ are considered on the same plot. Threshold voltage plot given in Fig 4.7 shows higher roll-off for recessed device as expected due to weaken control of gate on the channel. Similarly from Fig. 4.8 the increase in DIBL due to introduction of recessed-S/D portion is clear. However this small deterioration in SCE can be tolerated due to improvement of electrical properties of recessed-S/D structure.

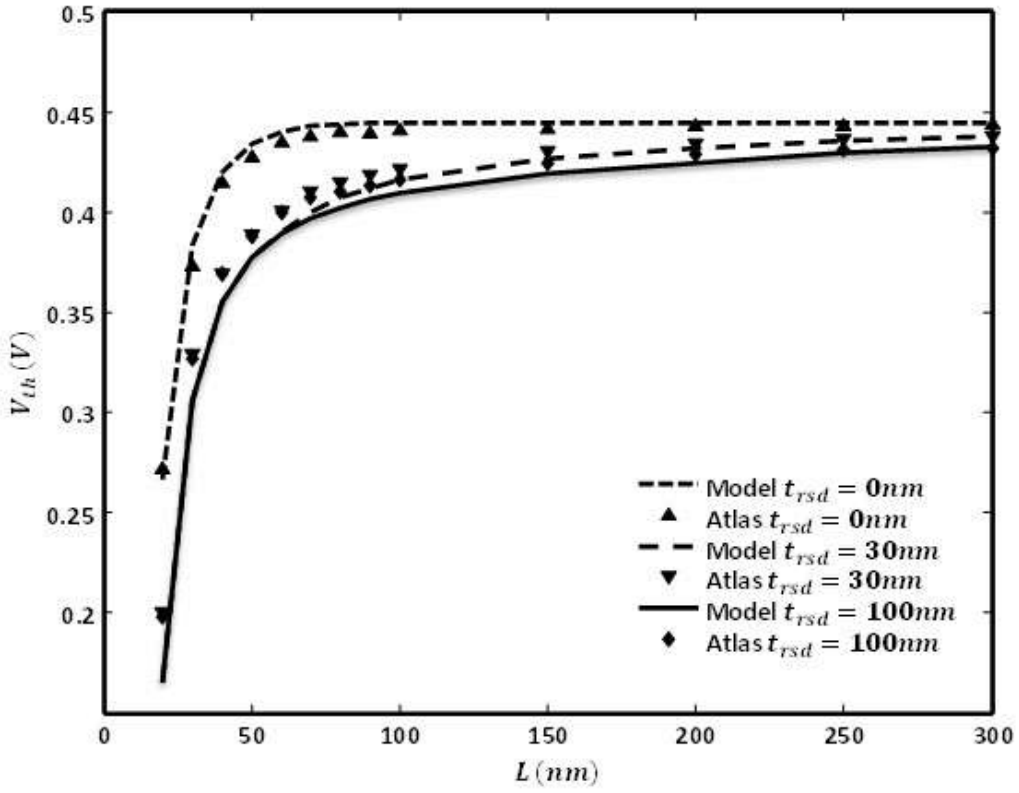

Figure 4.7: Threshold voltage (V_{th}) vs. channel length(L) at $t_{rsd} = 0, 30$ and 100nm with $t_{si} = 5nm$, $t_{ox} = 2nm$, $t_b = 200nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_d = 0.1V$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

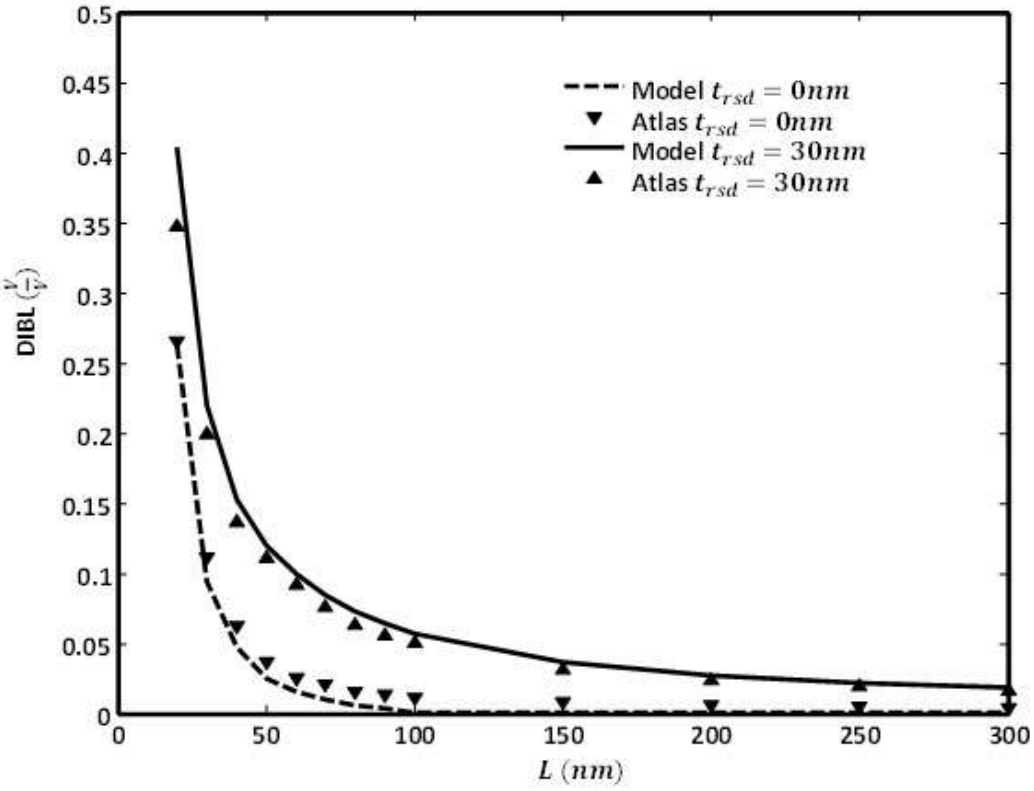

Figure 4.8: Threshold voltage (V_{th}) vs. channel length(L) at $t_{rsd} = 0nm$ and $30nm$ with $t_{si} = 5nm$, $t_{ox} = 2nm$, $t_b = 200nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

CHAPTER 5

SUBTHRESHOLD CHARACTERISTICS

5.1 Introduction

Subthreshold Characteristics of a MOS device is considered to be very important parameter for both analog and digital applications. It is easy to understand that, though MOS is a dc voltage controlled switch but drain current increases gradually with gate voltage instead of step increase.

The magnitude of drain current below threshold voltage is considered to be Subthreshold current. It is also named as subthreshold leakage, since it is not on current instead flow through drain without applying required gate bias.

Subthreshold current is basically weak inversion current and mostly degrade digital circuits made using MOS device. However, it can be useful in analog circuits to generate different functions [48].

The subthreshold slope is a measure of rate of increase of drain current with gate voltage subthreshold region of operation [27], [43] and [49]. It is measured on log scale as V/Decade and has ideal magnitude of 60.

5.2 Subthreshold Current and Subthreshold Slope Model

The subthreshold current density may be expressed as

$$J_n(x) = qD_n \frac{n_{min}(x)}{L_e} \left(1 - e^{\frac{V_{ds}}{V_T}}\right) \tag{5.1}$$

where D_n is electron diffusion constant, $n_{min}(x)$ is the minimum free electron density at $(x,\ y_{min})$ coordinate in channel, L_e is effective length of channel being calculated as [43] and [50], and V_T is thermal voltage. The expression of $n_{min}(x)$ is given by

$$n_{min}(x) = \frac{{n_i}^2}{N_a}\left(e^{\frac{\varphi(x,y_{min})}{V_T}}\right) \tag{5.2}$$

here, $\varphi(x, y_{min})$ is the minimum channel potential along channel length.

The subthreshold slope is characterized as the inverse of rate of increase of drain current with respect to gate voltage in the subthreshold region of operation [43] and [50]. It has been earlier proved that in the present model at low doping back channel controls the device operation while at high doping front surface is dominant. Following this finding subthreshold slope of Re-S/D SOI MOSFET may be defined by the following equation.

$$S = \begin{cases} \left.\frac{\ln(10)\cdot kT}{q}\cdot\frac{\partial\varphi(x,y_{min})}{\partial V_g}\right|_{x=0} & for,\ \varphi(0,y_{min}) > \varphi(t_{si},y_{min}) \\ \left.\frac{\ln(10)\cdot kT}{q}\cdot\frac{\partial\varphi(x,y_{min})}{\partial V_g}\right|_{x=t_{si}} & for,\ \varphi(0,y_{min}) < \varphi(t_{si},y_{min}) \end{cases} \tag{5.3}$$

The minimum of surface potential along the channel length $\varphi(x, y_{min})$ can be found from Eqs. (3.14) and (3.25). Eq. (3.25) being differentiated and equated to Zero to find y_{min}. Further substitution of y_{min} in Eq. (3.25) results in the following expression.

$$\varphi(x, y_{min}) = V(x) + U(x, y_{min}) \tag{5.4}$$

and

$$U(x, y_{min}) = 2\sqrt{QR}\cdot[\cos(\lambda x) + P\cdot sin(\lambda x)] \tag{5.5}$$

where P, Q, R, and λ are taken from Eqs. (3.26), (3.27), (3.28) and (3.22) respectively.

Thus subthreshold current per unit channel width can be obtained using Eq. (5.4) into Eq. (5.1) and subsequent integration as

$$I_{ds} = \int_0^{t_{si}} J_n(x)dx \tag{5.6}$$

Since, $\varphi(x, y_{min})$ is a function of ΔV and ΔV is itself a function of V_g hence rigorous mathematical derivation is required to find $\frac{d\,\varphi(x,y_{min})}{d\,V_g}$ in explicit form. However the same can be solved fairly using Eqs. (3.38), (3.15) and (3.16). From Eq. (3.14) and Eq. (5.5) the following can be obtained

$$\frac{dV(x)}{dV_g} = \left\{\frac{C_{ox}C_{si}}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)} + \frac{C_b(C_{si}+C_{ox})}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)}\frac{d\Delta V}{dV_g}\right\}\frac{x}{t_s} +$$

$$\left\{\frac{C_{ox}(2C_r+C_b+C_{si})}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)} + \frac{C_bC_{si}}{C_{ox}C_{si}+(C_{si}+C_{ox})(2C_r+C_b)}\frac{d\Delta V}{dV_g}\right\}\left(1-\frac{x}{t_s}\right) \quad (5.7)$$

and

$$\frac{dU(x,y_{min})}{d\,V_g} = \frac{1}{e^{\lambda L}-e^{-\lambda L}}\left[\sqrt{\frac{R}{Q}}\left(e^{-\lambda L}-1\right)+\sqrt{\frac{R}{Q}}\left(1-e^{\lambda L}\right)\right]\frac{dV(x)}{dV_g} \quad (5.8)$$

Thus results $\frac{\partial\varphi(x,y_{min})}{\partial V_g}$ in Eq. (5.3) are given below

$$\frac{\partial\varphi(x,y_{min})}{\partial V_g} = \frac{dV(x)}{d\,V_g} + \frac{dU(x,y_{min})}{d\,V_g} \quad (5.9)$$

Thereafter using Eq. (5.9) into Eq. (5.3) the subthreshold slope can be obtained. The next sub section shows the numerical result with the help of plots.

5.3 Results and Discussion

Simulating Eq. (5.6) and Eq. (5.3) in Matlab, subthreshold current and subthreshold slope has been obtained for various device parameters. The Atlas simulation results have been plotted together with the model results to verify the accuracy of model.

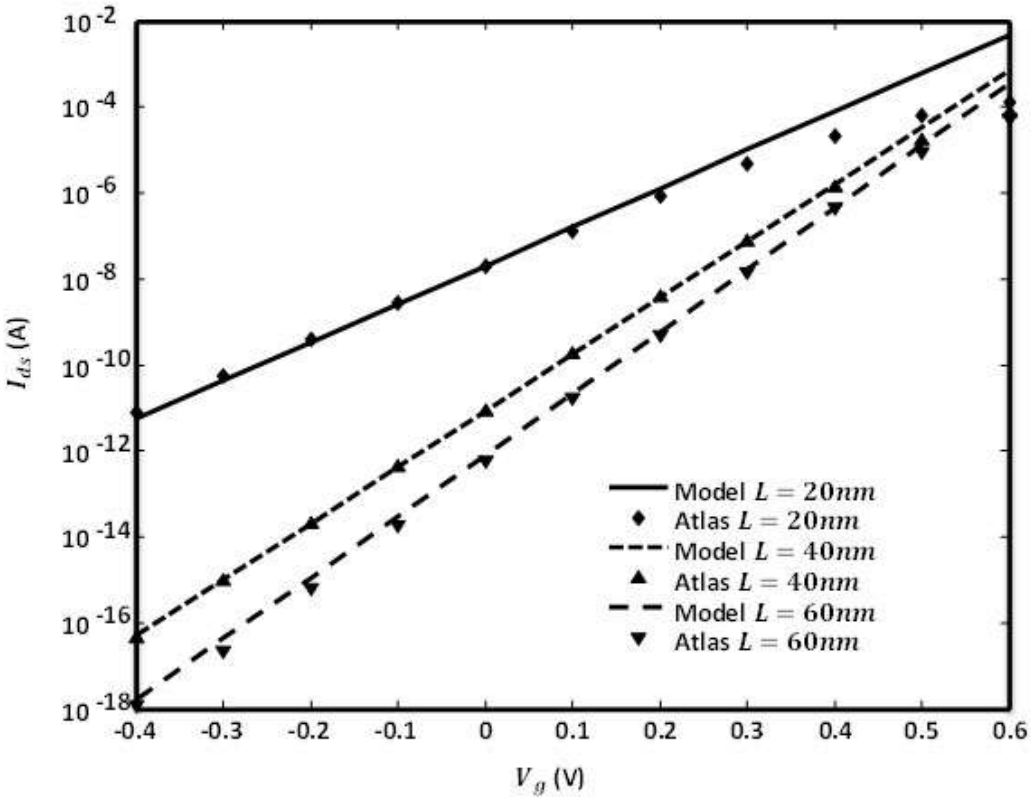

Figure 5.1: Subthreshold current (I_{ds}) vs. gate voltage(V_g) at $t_{si} = 5nm$, $t_{ox} = 2nm$, $t_b = 200nm$, $t_{rsd} = 30nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

Figure 5.1 shows subthreshold current vs. gate voltage plot for channel length of $20nm, 40nm$ and $60nm$. It can be observed that in the subthreshold region the model and simulation are in exact match while the two deviates from each other beyond gate voltage greater than threshold voltage. Also subthreshold current appears to be increasing with decrease in channel length and the plot shifts upward. It can be justified by the fact that at lower channel length gate control is diminished and leakage current increase.

Figure 5.2 shows subthreshold current vs. gate voltage plot at a channel length of $20nm$, but variation in channel thickness. Increase in leakage current due to higher channel area causes increase in subthreshold current. Thus subthreshold plot corresponding to $t_{si} = 10nm$ has moved up with respect to plot corresponding to $t_{si} = 5nm$. Hence for digital applications where subthreshold current poses major challenge due to power dissipation the channel thickness should be minimum.

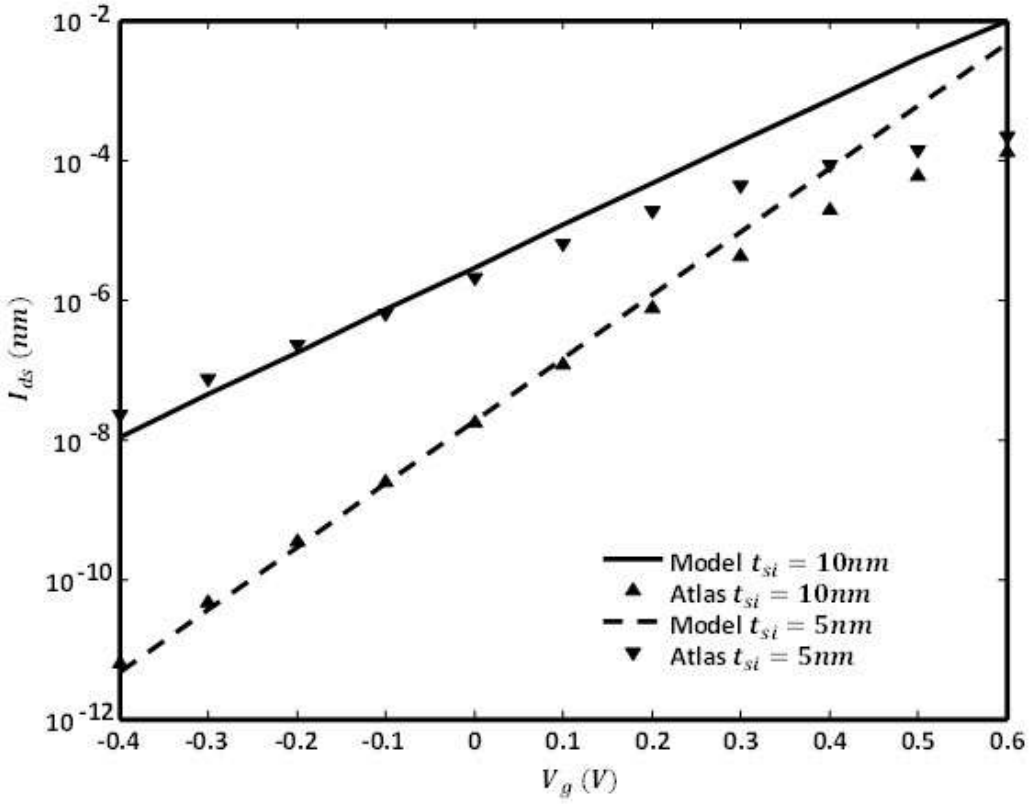

Figure 5.2: Subthreshold current (I_{ds}) vs. gate voltage(V_g) at $t_{si} = 5nm$ and $t_{si} = 10nm$ with $L = 20nm$, $t_{ox} = 2nm$, $t_b = 200nm$, $t_{rsd} = 30nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

Figure 5.3 demonstrate the effect of gate-oxide thickness variation on subthreshold current. The channel length is assumed to be constant and equal to $20nm$. From the figure it can be observed that with the increase in gate-oxide thickness the subthreshold current increases. It can be explained by the fact that due to increase in gate-oxide thickness the control of gate over channel decreases. Hence gate-oxide thickness of $2nm$ is preferred over $5nm$. But the gate-oxide thickness reduction beyond a limit causes gate-tunneling, hence a balance should be maintained.

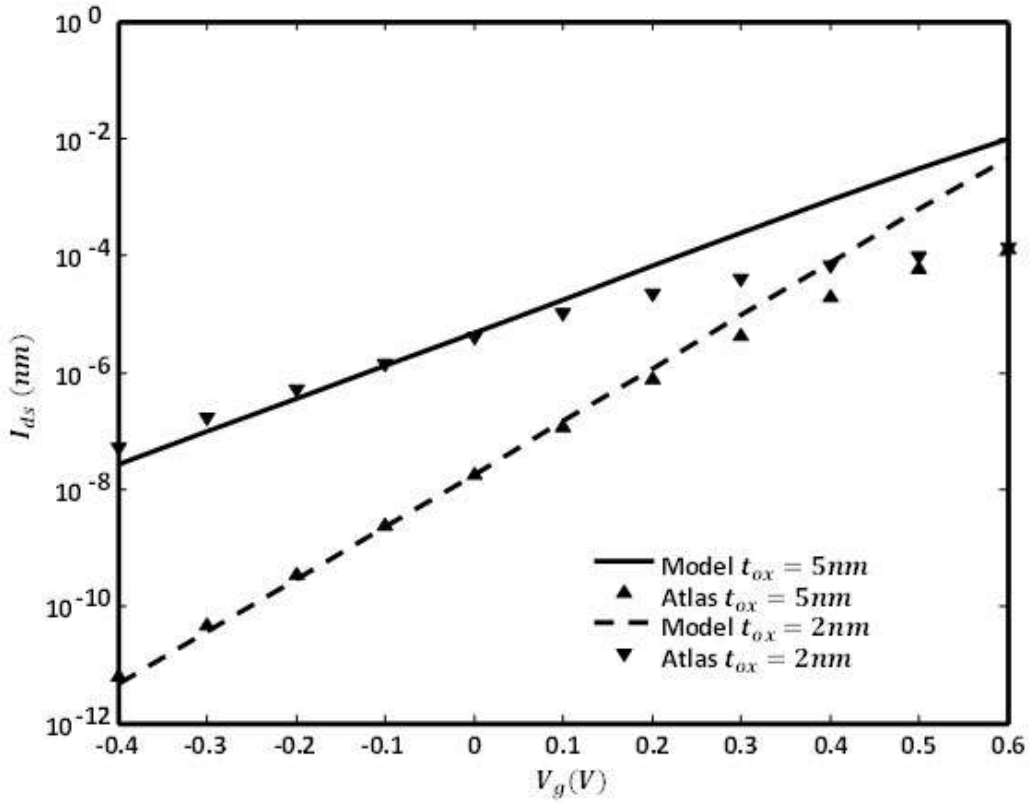

Figure 5.3: Subthreshold current (I_{ds}) vs. gate voltage(V_g) at $t_{ox} = 2nm$ and $t_{ox} = 5nm$ with $L = 20nm$, $t_{si} = 5nm$, $t_b = 200nm$, $t_{rsd} = 30nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

Lastly, a subthreshold slope characteristic is being shown in Figure 5.4. It shows subthreshold slope versus channel length while rest of the parameters are mentioned in the figure caption. The sharp increase in slope with decrease in channel length can be observed easily. It is a drawback of device scaling. Further it is clear that at a thinner channel the subthreshold slope decreases. Hence it can be said that a proportional scaling in channel thickness can control the drastic increase in slope during scaling the device.

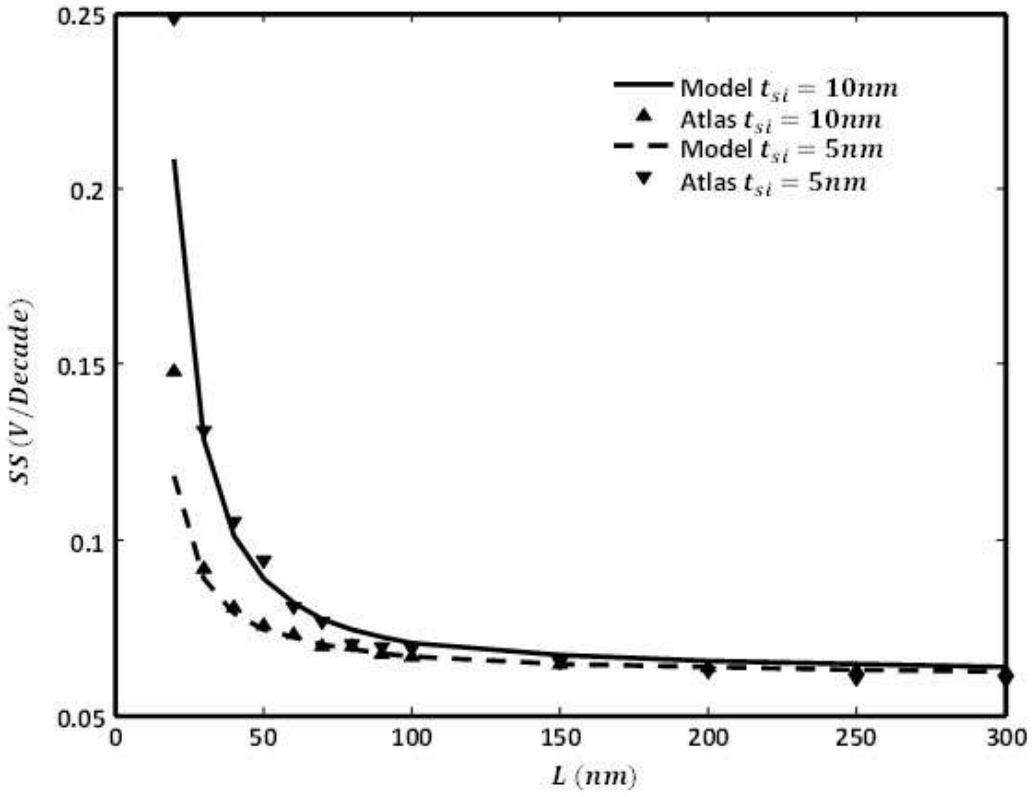

Figure 5.4: Subthreshold slope (SS) vs. Channel length(L) at $t_{si} = 5nm$ and $t_{si} = 10nm$ with $L = 20nm$, $t_{ox} = 2nm$, $t_b = 200nm$, $t_{rsd} = 30nm$, $N_a = N_{sub} = 10^{15}cm^{-3}$, $N_d = N_s = 10^{20}cm^{-3}$, $V_{sub} = 0V$, and $\phi_M = 4.8eV$.

CHAPTER 6

CONCLUSION

The surface potential, threshold voltage and subthreshold characteristic of short-channel FD Re-S/D UTB SOI MOSFETs have been modeled using Evanescent mode analysis. Modeling of substrate induced surface potential effects for the device was carried out and was included in the device model to improve the accuracy of device characteristics. It is found that at low channel doping back surface of the channel dominates the current flow while at higher channel doping front surface of the channel becomes dominant. Also it was found that the SISP effect is dominant in inversion region of the substrate while in accumulation region it can be neglected. The study of SCE with channel thickness, gate-oxide thickness and recessed-S/D depth were carried out to improve the device performance. The device modeling results were plotted with the ATLAS simulation up to 20nm channel length and model results were found to be in excellent agreement with ATLAS simulation.

Based on the success of the model for Re-S/D SOI MOSFET, its performance up to 10nm and below can be tested using quantum confinement simulation in ATLAS also the performance optimization can be carried out to discover the future scope of the device.

LIST OF REFERENCES

[1] V.M. Masson, The Bronze Age in Khorasan and Transoxiana, chapter 10 in A.H. Dani and Vadim Mikhaĭlovich Masson (eds.), History of civilizations of Central Asia, volume 1: The dawn of civilization: earliest times to 700 BC.

[2] Amélie Kuhr. The Ancient Near East, c. 3000–330 BC. Page 9.

[3] G. Busch, "Early history of physics and chemistry of semiconductor- from doubts to facts in a hundred years", European J. of Physics, Vol. 10, No. 4, pp. 254-262, 1989.

[4] L. Lukasiak, and A. Jakubowski, "History of Semiconductor", Journal of Telecommunication and Information Technology, pp. 3-9, Jan 2010.

[5] E. Mollick, "Establishing Moore's law," IEEE Annals of the history of computing, Vol. 6, pp. 62-73, 2006.

[6] R. H. Dennard, F. H. Gaensslen, L. Kuhn, N. Y. Yu, V. L. Ridout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," IEEE J. Solid-State Circuits, Vol. 9, pp. 256–268, 1974.

[7] R. H. Dennard, F. H. Gaensslen, L. Kuhn, N. Y. Yu, V. L. Ridout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," IEEE J. Solid-State Circuits, vol. SC-9, pp. 256–268, 1974.

[8] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," IEEE Trans. Electron Devices, vol. ED-31, pp. 452–462, 1984.

[9] A. G. Sabnis and J. T. Clemens, “Characterization of the electron mobility in the inverted <100> Si surface,” in IEDM Tech. Dig., pp. 18–21, 1979.

[10] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, “On the universality of inversion-layer mobilty in Si MOSFETs. Part I- Effect of substrate impurity concentration,” IEEE Trans. Electron Devices, vol. 41, pp. 2357–62, Dec. 1994.

[11] T. Mizuno, J. Okamura, and A. Toriumi, “Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFETs”, IEEE Trans. on Electron Devices, Vol. 41, No. 11, pp. 2216-2221, Nov. 1994.

[12] E. Suzuki, K. Ishii, S. Kanemaru, T. Tsutsumi, T. Sekigawa, K. Nagai, and H. Hiroshima, “Highly suppressed short channel effects in ultrathin SOI n-MOSFETs,” IEEE Trans. On Electron Device, Vol. 47, No. 2, pp. 453-357, Feb. 2000.

[13] H. Wang, M. Chan, Y. Wang, and P. K. Ko, “The Behavior of narrow-width SOI MOSFETs with mesa isolation,” IEEE Trans. On Electron Device, Vol. 47, No. 3, pp. 593-562, Mar. 2000.

[14] Y. K. Choi, K. Asano, N. Lindert, V. Subramanian, T.J. King, J. Bokor, and C. Hu, “Ultrathin-body SOI MOSFET for deep-sub-tenth micron era” IEEE Electron Device Letters, Vol. 21, No. 5, pp. 254-255, May 2000.

[15] D. Esseni, A. Abramo, L. Selmi, and E. Sangiorgi, “Physically Based Modeling of Low Field Electron Mobility in Ultrathin Single- and Double-Gate SOI n-MOSFETs,” IEEE Trans. On Electron Devices, Vol. 50, No. 12, pp. 2445-2454, Dec. 2003.

[16] A. O. Adan, K. Higashi, and Y. Fukushima, “Analytic threshold voltage model for ultrathin SOI MOSFETs including short channel and floating body effects,” IEEE Trans. On Electron Device, Vol. 46, No. 4, pp. 729-733, Apr. 1999.

[17] A. Majumdar, Z. Ren, J. W. Sleight, D. Dobuzinsky, J. R. Holt, R. Venigalla, S. J. Koester, and W. Haensch, "High-performance undoped-body 8-nm-thin SOI field-effect transistors," IEEE Electron Device Letters, Vol. 29, No. 5, pp. 515-517, May 2008.

[18] S. M. Ramey, and D. K. Ferry, "Threshold voltage calculation in ultrathin film SOI MOSFETs using the effective potential," IEEE Trans. On Nanotechnology, Vol. 2, No. 3, pp. 121-124, 2003.

[19] S. M. Ramey, and D. K. Ferry, "Modeling of quantum effects in ultrasmall FD-SOI MOSFETs with effective potentials and 3D Monte Carlo," Ohys. B: Condens Matter, Vol. 314, pp. 350-353, Mar. 2002.

[20] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum mechanical effects on the threshold voltage of ultrathin SOI nMOSFETs," IEEE Elect. Device Letter, Vol. 14, pp. 569-572, Dec. 1993.

[21] D. Ranka, A. K. Rana, R. K. Yadav, K. Yadav, D. Giri, "Performance evaluation of FD-SOI MOSFETs for different metal gate work function," International Journal of VLSI design & Communication Systems, Vol.2, No.1, pp. 11-24, March 2011.

[22] T. Sakurai, A. Matsuzawa and T. Douseki, "Fully-Depleted SOI CMOS circuits and technology for ultralow-power applications," Springer, 2006.

[23] T. Tsuchiya, Y. Sato, and M. Tomizawa, "Three mechanisms Determining Short-Channel Effects in Fully Depleted SOI MOSFETs," IEEE Trans. Electron Devices, Vol. 45, pp. 1116–1121, May 1998.

[24] Z. Zhang, S. Zhang, and M. Chan, "Self-Align recessed source drain ultrathin body SOI MOSFET," IEEE Electron Dev. Letters, Vol. 25, No. 11, Nov. 2004.

[25] B. Svilicic, V. Jovanovic, T. Suligoj, “Analytical models of front- and back-gate potential distribution and threshold voltage for recessed source/drain UTB SOI MOSFETs,” Solid-State Electron, Vol. 53, pp. 540-547, 2009

[26] W. Ke, X. Han, D. Li, X. Wang, R. Han, T. Zhang, R. Han, and S. Zhang “Recessed source/drain for sub-50nm UTB SOI MOSFET,” Semiconductor Sci. and Technol., Vol. 22, pp. 577-583, 2007.

[27] B. Svilicic, V. Jovanovic, and T. Suligoj, “Analysis of subthreshold conduction in short-channel recessed source/drain UTB SOI MOSFETs” , Solid-State Electron, Vol. 54, pp. 545-551, 2010.

[28] V. P. Trivedi, and J. G. Fossum, “Quantum-mechanical effects on the threshold voltage of undoped double-gate MOSFETs”, IEEE Elec. Device Letters, Vol. 26, No. 8, pp. 579-582, Aug. 2005.

[29] L. Ge, and J. G. Fossum, “Analytical modeling of quantization and volume inversion in thin Si-film double-gate MOSFETs,” IEEE Trans. Electron Devices, Vol. 49, No. 2, pp. 287-294, Feb. 2002.

[30] J. W. Yang, and J. G. Fossum, “On the feasibility of nanoscale triple-gate CMOS transistors”, IEEE Trans. Electron Devices, Vol. 52, No. 3, pp. 1159-1164, Jun. 2005.

[31] David Russell Evans, and Sheng Teng Hsu, “Fabrication of a planar MOSFET with raised source/drain by chemical mechanical polishing and nitride replacement,” Publication number US6133106 A, Oct. 2000.

[32] V. Y. Thean, B. J. Goolsby, B. Y. Nguyen, T. T. Nguyen, and T. A. Stephens, “Semiconductor fabrication process including recessed sourec/drain regions in an SOI wafer,” Patent No. US 7091071 B2, Aug. 2006.

[33] J. Kedzierski, P. Xuan, V. Subramanian, J. Bokor, T. J. King, and C. Hu, "A 20-nm gate-length ultra-thin body p-MOSFET with silicide source/drain," Superlattices and Microstructures, Vol. 28, pp. 445-452, No. 5/6, 2000.

[34] Z. Zhang, S. Zhang, M. Chan, "Self-Align recessed source drain ultrathin body SOI MOSFET," IEEE Electron Device Letters, Vol. 25, No. 11, Nov. 2004.

[35] G. Wang, K. Cheng, J. Ervin, C. Pie, and R. M. Todi, "Recessed single crystalline source and drain for Semiconductor-on-insulator devices," Pub. No. US 2013/0105898A1, May 2013

[36] C. G. Ahn, W. J. Cho, K. J. Im, J. H. Yang, I. B. Baek, S. K. Baek, and S. J. Lee, "Recessed source-drain(S/D) SOI MOSFETs with low S/D extension (SDE) external resistance," IEEE International SOI Conference, pp. 207-208, 2004.

[37] W. Ke, X. Han, D. Li, X. Wang, R. Han, T. Zhang, R. Han, and S. Zhang "Recessed source/drain for sub-50nm UTB SOI MOSFET," Semiconductor Sci. and Technol., Vol. 22, pp. 577-583, 2007

[38] W. Ke, X. Han, D. Li, X. Wang, R. Han, T. Zhang, R. Han, and S. Zhang "Recessed source/drain for scaling SOI MOSFET to the limit," International Conf. on Solid-State and Integrated Circuit Technology(ICSICT) , pp. 84 - 86, 2006.

[39] W. Ke, S. Zhang, X. Liu, and R. Han, "Sorurce/Drain resistance of UTB SOI MOSFET," IEEE Conference on Electron Devices and Solid-State Circuits, pp. 405 – 408, 2005.

[40] C. G. Ahn, W. J. Cho, K. Im, J. H. Yang, I. B. Baek, S. Baek, and S. Lee, "30-nm recessed S/D SOI MOSFET with an Ultrathin body and a low SDE resistance," IEEE Electron Dev. Letters, Vol. 26, No. 7, pp. 486-488, 2005.

[41] S. S. Tan, S. Fang, J. Yuan, L. Zhao, Y. M. Lee, J. J. Kim, R. Robinson, J. Yan, J. Park, M. Belyansky, J. Li, R. Stierstorfer, S. D. Kim, N. Rovedo, H. Shang, H. Ng, Y. Li, J. Sudijono, E.

Quek, S. Chu, R. Divakaruni, and S. Iyer “Enhanced Stress Proximity Technique with Recessed S/D to improve device performance at 45nm and beyond,” International Symposium on VLSI Technology, Systems and Applications, pp. 122-123, 2008.

[42] J. Kedzierski, P. Xuan, V. Subramanian, J. Bokor, T. J. King, and C. Hu, “A 20-nm gate-length ultra-thin body p-MOSFET with silicide source/drain,” Superlattices and Microstructures, Vol. 28, pp. 445-452, No. 5/6, 2000.

[43] G.K. Saramekala, A. Santra, M. Kumar, S. Dubey, S. Jit, and P.K. Tiwari, “Analytical subthreshold current and subthreshold swing models of short-channel dual-metal-gate (DMG) fully-depleted recessed-source/drain (Re-S/D) SOI MOSFETs,” Journal of Computational Electronics, Feb. 2014

[44] M. A. Imam, M. A. Osman, and A. A. Osman, “Threshold voltage model for deep-submicron fully depleted SOI MOSFETs with back gate substrate induced surface potential effects,” Microelectronics Reliability, Vol. 39, pp. 487-495, Jan. 1999.

[45] J. H. Sim, and J. B. Kuo, “An analytical back-gate bias effect model for ultrathin SOI CMOS devices,” IEEE Trans Electron Devices, Vol. 40, No. 4, pp. 755-765, Apr. 1993.

[46] C. T. Lee, and K. K. Young, “Sub-micrometer near-intrinsic thin-film SOI complementary MOSFET’s,” IEEE Trans Electron Devices, Vol. 36, No. 11, pp. 2537-2547, Nov. 1989.

[47] Q. Chen, “Scaling limits and opportunities of Double-gate MOSFET,” Ph D thesis, Georgia Institute of Technology, 2003.

[48] Eric A. Vittoz, "The Fundamentals of Analog Micropower Design," John Wiley and Sons. pp. 365–372, 1996.

[49] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, "FDSOI process technology for subthreshold operation ultralow power electronics," IEEE Proceeding, Vol.98, No. 2, pp. 333-338, Feb. 2010.

[50] A. Dey, A. Chakravorty, N. Dasgupta, and A. Dasgupta, "Analytical model of subthreshold current and slope for asymmetric 4-T and 3-T double-gate MOSFETs," IEEE Trans. On Electron Device, Vol. 55, No. 12, pp. 3442-3448, 2008.

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